

TN9926CNPA

Dual N-Channel Enhancement Mode Power MOSFET

Product Summary

- V_{DS}= 20V,I_D= 4A
- $R_{DS(on)}$ < 55m Ω @ V_{GS} = 4.5V
- $R_{DS(on)} < 85 \text{m}\Omega @V_{GS} = 2.5V$

Features

- Advanced Trench Technology
- RoHS and Reach Compliant
- Halogen and Antimony Free
- Moisture Sensitivity Level 3

Application

- Power Switching Application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

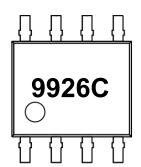
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SOP-8

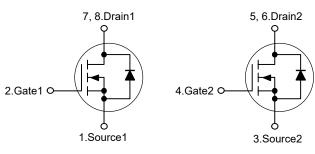
(Top View)

Pin	Description	Pin	Description
1	Source1	4	Gate2
2	Gate1	5,6	Drain2
3	Source2	7,8	Drain1

Marking Code



Schematic Diagram



N-Channel

N-Channel

Absolute Maximum Ratings

Ratings at 25°C ambient temperature unless otherwise specified.

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±12	V
Drain Current-Continuous	I _D	4	А
Drain Current-Pulsed Note1	I _{DM}	21	Α
Maximum Power Dissipation	P _D	2.0	W
Junction Temperature	TJ	150	°C
Storage Temperature Range	T _{STG}	-55 to +150	°C

Thermal Characteristics

Thermal Resistance,Junction-to-Ambient Note2	R _{0JA}	62.5	°C/W
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Electrical Characteristics

(T_J=25°C unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	20			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.044		V/°C	Reference to 25°C, I _D = 1mA
				0.050		V _{GS} = 4.5V, I _D = 2.6A ③
R _{DS(ON)}	Static Drain-to-Source On-Resistance			0.070	Ω	V _{GS} = 2.7V, I _D = 2.2A ③
$V_{GS(th)}$	Gate Threshold Voltage	0.70			V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
g _{fs}	Forward Transconductance	8.3			S	V _{DS} = 15V, I _D = 2.6A
	Durin to Comment			1.0		V _{DS} = 16V, V _{GS} = 0V
I _{DSS}	Drain-to-Source Leakage Current			25	μΑ	V _{DS} = 16V, V _{GS} = 0V, T _J = 125 °C
1	Gate-to-Source Forward Leakage			100	nA	V _{GS} = 12V
I _{GSS}	Gate-to-Source Reverse Leakage			-100	nA	V _{GS} = - 12V
Qg	Total Gate Charge			20		I _D = 2.6A
Q _{gs}	Gate-to-Source Charge			2.2	nC	V _{DS} = 16V
Q _{qd}	Gate-to-Drain ("Miller") Charge			8.0		V _{GS} = 4.5V, See Fig. 6 and 12 ③
t _{d(on)}	Turn-On Delay Time		9.0			V _{DD} = 10V
t _r	Rise Time		42			I _D = 2.6A
t _{d(off)}	Turn-Off Delay Time		32		ns	$R_G = 6.0\Omega$
t _f	Fall Time		51			R_D = 3.8 Ω , See Fig. 10 ③
L _D	Internal Drain Inductance		4.0		nH	Between lead tip
L _S	Internal Source Inductance	_	6.0		''''	and center of die contact
C _{iss}	Input Capacitance		660			V _{GS} = 0V
Coss	Output Capacitance		280		pF	V _{DS} = 15V
C _{rss}	Reverse Transfer Capacitance		140			f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Тур.	Max.	Units	Conditions
Is	Continuous Source Current			2.5		MOSFET symbol
	(Body Diode)			2.5	Α	showing the
I _{SM}	Pulsed Source Current			24	^	integral reverse
Ī	(Body Diode) ①			21		p-n junction diode.
V_{SD}	Diode Forward Voltage			1.0	V	$T_J = 25^{\circ}C$, $I_S = 1.8A$, $V_{GS} = 0V$ ③
t _{rr}	Reverse Recovery Time		29	44	ns	$T_J = 25^{\circ}C$, $I_F = 2.6A$
Q_{rr}	Reverse RecoveryCharge		22	33	nC	di/dt = 100A/µs ③
ton	Forward Turn-On Time	Intri	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)			

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- $\begin{tabular}{ll} \textcircled{2} & I_{SD} \leq 2.6A, \ di/dt \leq 100A/\mu s, \ V_{DD} \leq V_{(BR)DSS}, \\ & T_{J} \leq 150 \ensuremath{^{\circ}C} \ensuremath{C} \ensuremath{C} \ensuremath{D}$
- 4 Surface mounted on FR-4 board, $t \le 10$ sec.

Typical Characteristic Curves

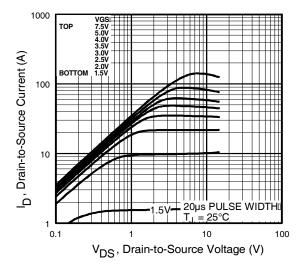
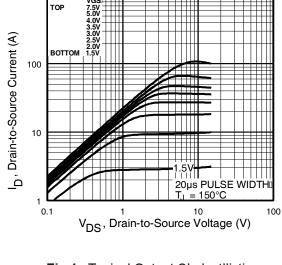


Fig 1. Typical Output Characteristics



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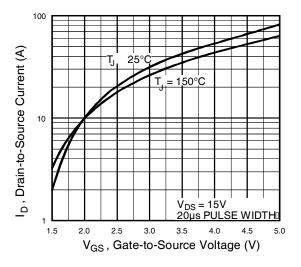


Fig 3. Typical Transfer Characteristics

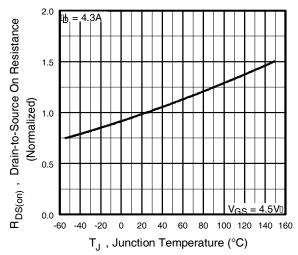


Fig 4. Normalized On-Resistance Vs. Temperature

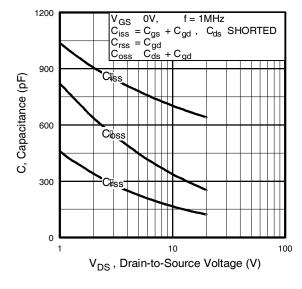


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

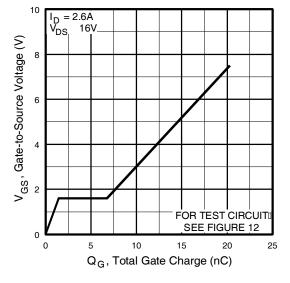


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

Typical Characteristic Curves

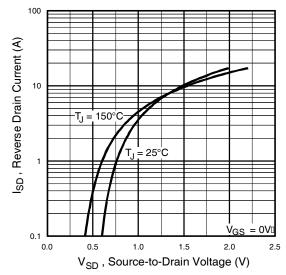


Fig 7. Typical Source-Drain Diode Forward Voltage

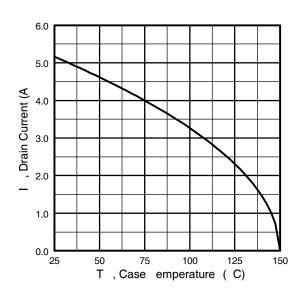


Fig 9. Maximum Drain Current Vs.
Ambient Temperature

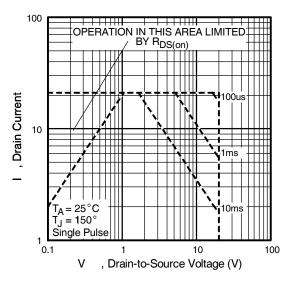


Fig 8. Maximum Safe Operating Area

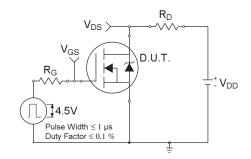


Fig 10a. Switching Time Test Circuit

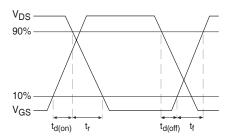


Fig 10b. Switching Time Waveforms

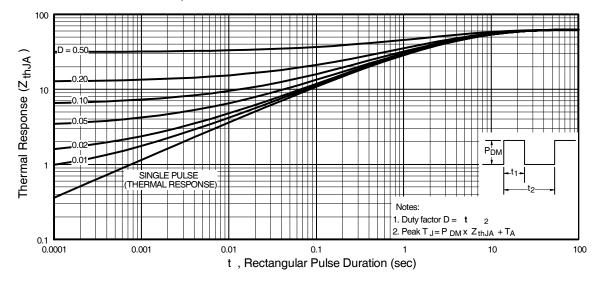
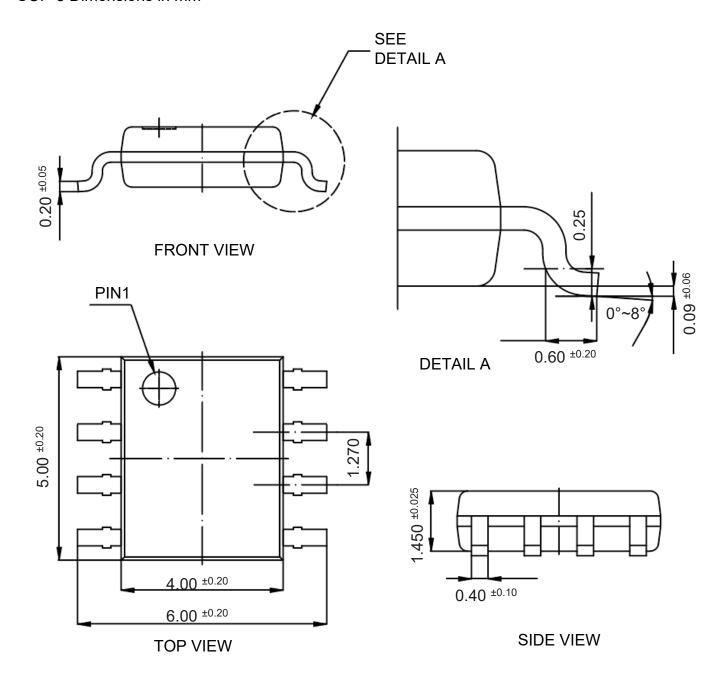


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Package Outline

SOP-8 Dimensions in mm



Ordering Information

Device	Package	Shipping
TN9926CNPA	SOP-8	4,000PCS/Reel&13inches

Contact Information

For additional information, please contact your local Sales Representative.



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