

TN70P30DL

P-Channel Enhancement Mode Power MOSFET

Product Summary

- $V_{DS} = -30V, I_D = -70A$
- $R_{DS(on)} < 10m\Omega @ V_{GS} = -10V$
- $R_{DS(on)} < 14m\Omega @ V_{GS} = -4.5V$

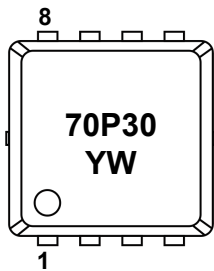
Features

- Advanced Trench Technology
- 100% Avalanche Tested
- RoHS Compliant
- Halogen and Antimony Free
- Moisture Sensitivity Level 3

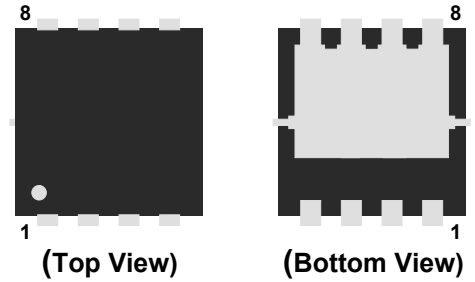
Application

- Lithium Battery Protection
- Wireless Impact
- Mobile Phone Fast Charging

Marking Code

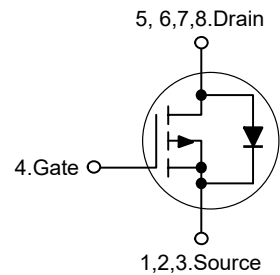


PDFN3x3-8L



Pin	Description
1,2,3	Source
4	Gate
5,6,7,8	Drain

Schematic Diagram



Absolute Maximum Ratings

Ratings at 25°C case temperature unless otherwise specified.

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	-70	A
$I_D @ T_C = 75^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	-35	A
IDM	Pulsed Drain Current ²	-175	A
EAS	Single Pulse Avalanche Energy ³	31	mJ
$P_D @ T_C = 25^\circ C$	Total Power Dissipation ⁴	31.2	W
TSTG	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	4	°C/W

Electrical Characteristics

(T_C=25°C unless otherwise specified)

Drain-Source Breakdown Voltage		V _(BR) DSS	V _{GS} = 0V, I _D = -250μA	-30	-	-	V
Gate-body Leakage current		I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T _J =25°C	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V	-	-	-1	μA
	T _J =55°C			-	-	-5	
Gate-Threshold Voltage		V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.0	-1.6	-2.5	V
Drain-Source On-Resistance ²		R _{DS(on)}	V _{GS} = -10V, I _D = -12A	-	6.5	9.3	mΩ
			V _{GS} = -4.5V, I _D = -8A	-	9.5	14.5	
Forward Transconductance		g _{fs}	V _{DS} = -5V, I _D = -20A	-	28	-	S
Dynamic Characteristics							
Input Capacitance		C _{iss}	V _{DS} = -15V, V _{GS} =0V, f =1MHz	-	4320	-	pF
Output Capacitance		C _{oss}		-	529	-	
Reverse Transfer Capacitance		C _{rss}		-	487	-	
Switching Characteristics							
Gate Resistance		R _g	V _{DS} = 0V, V _{GS} = 0V, f=1.0MHz	-	4.0	-	Ω
Total Gate Charge		Q _g	V _{GS} = -10V, V _{DS} = -15V, I _D = -15A	-	45	-	nC
Gate-Source Charge		Q _{gs}		-	8.5	-	
Gate-Drain Charge		Q _{gd}		-	12.8	-	
Turn-On Delay Time		t _{d(on)}	V _{GS} = -10V, V _{DD} = -15V, R _G = 2.5Ω, I _D = -15A	-	18.9	-	nS
Rise Time		t _r		-	15.7	-	
Turn-Off Delay Time		t _{d(off)}		-	64.8	-	
Fall Time		t _f		-	36.5	-	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ²		V _{SD}	I _S = -1A, V _{GS} = 0V	-	-	-1	V
Continuous Source Current ^{1,5}		I _S	V _G =V _D =0V , Force Current	-	-	-65	A

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V_{DD}= -25V, V_{GS}= -10V, L= 0.1mH, I_{AS}= -25A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics Curves

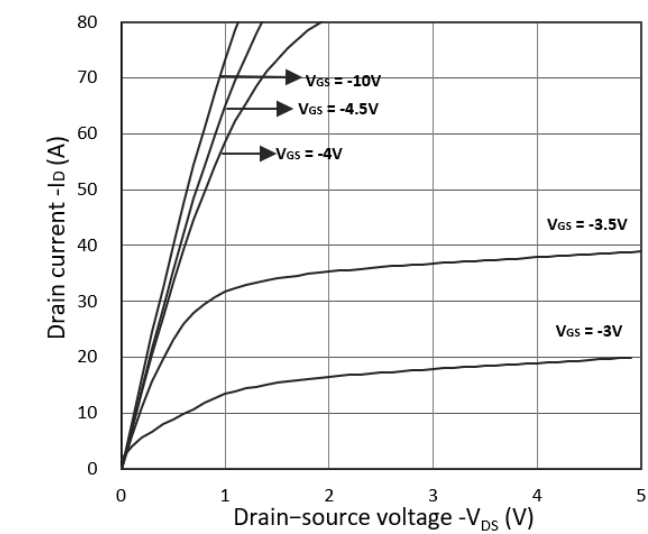


Figure 1. Output Characteristics

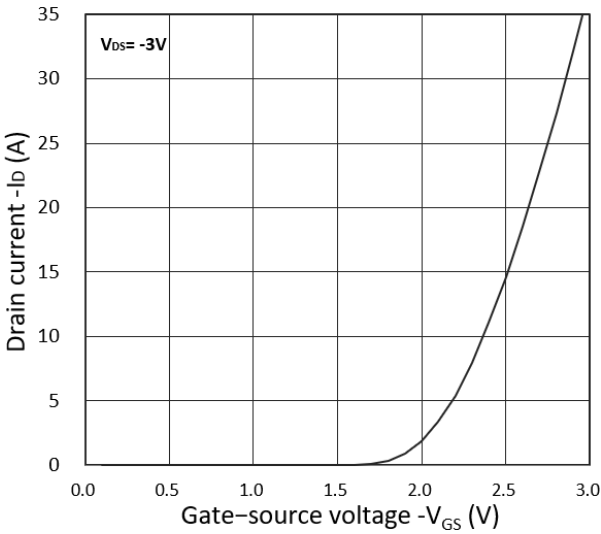


Figure 2. Transfer Characteristics

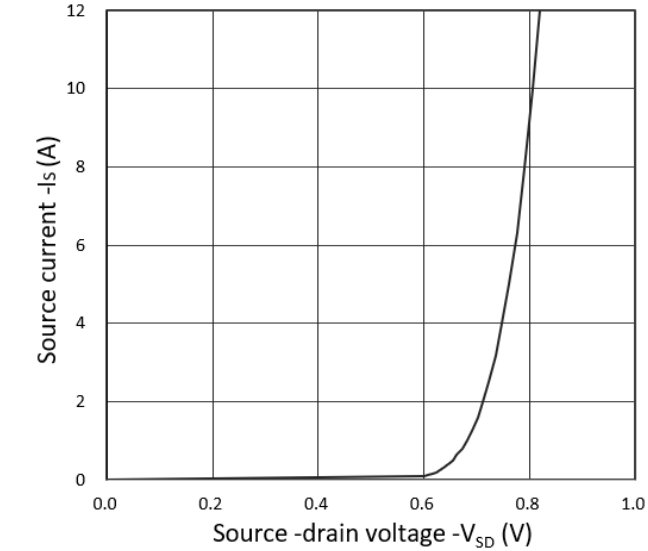


Figure 3. Forward Characteristics of Reverse

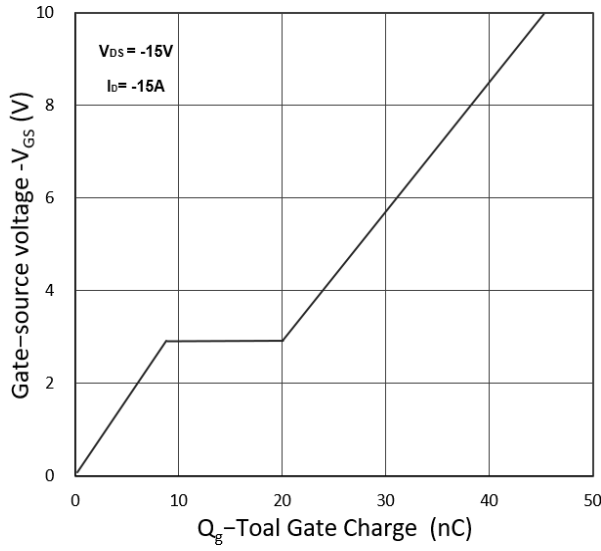


Figure 4. Gate Charge Characteristics

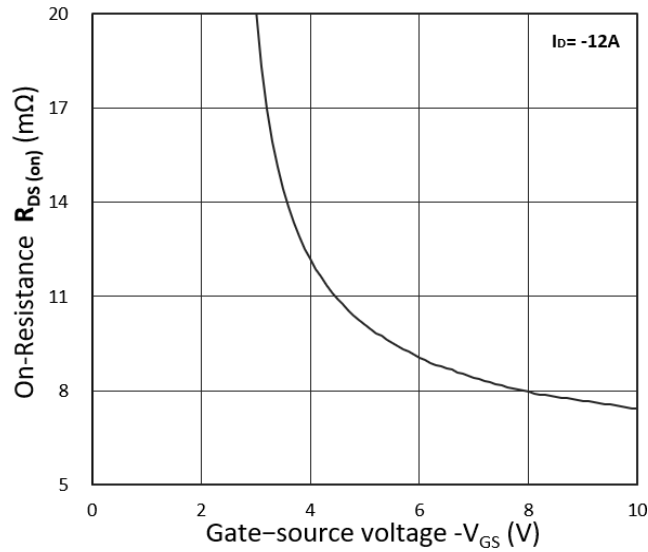


Figure 5. $R_{DS(on)}$ vs. V_{GS}

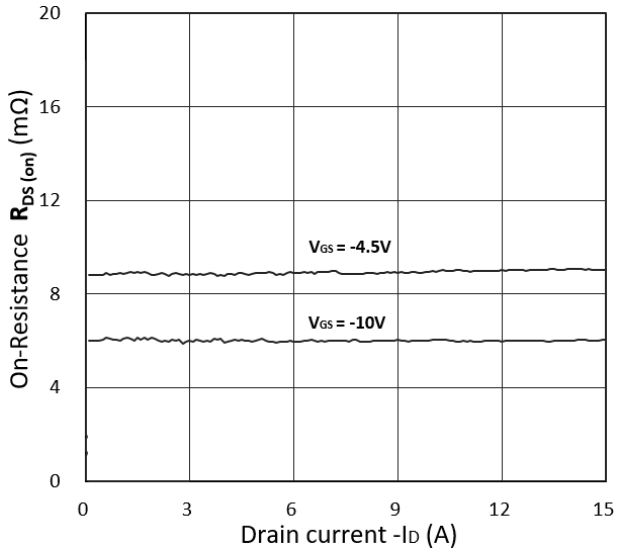


Figure 6. $R_{DS(on)}$ vs. I_D

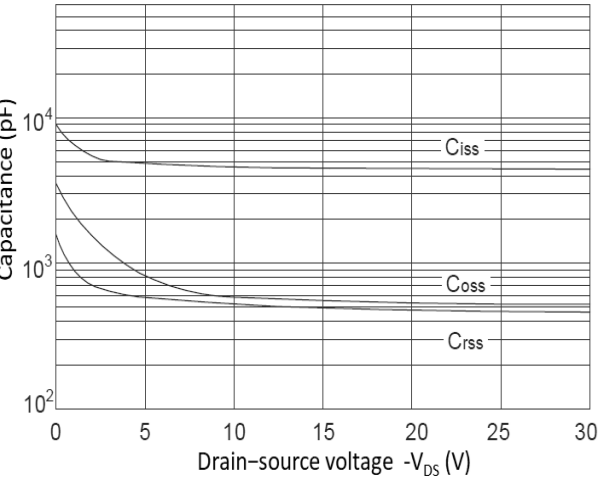


Figure 7. Capacitance Characteristics

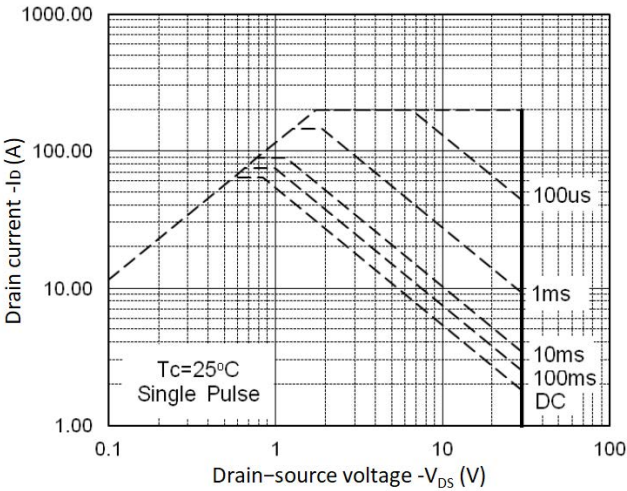


Figure 8. Safe Operating Area

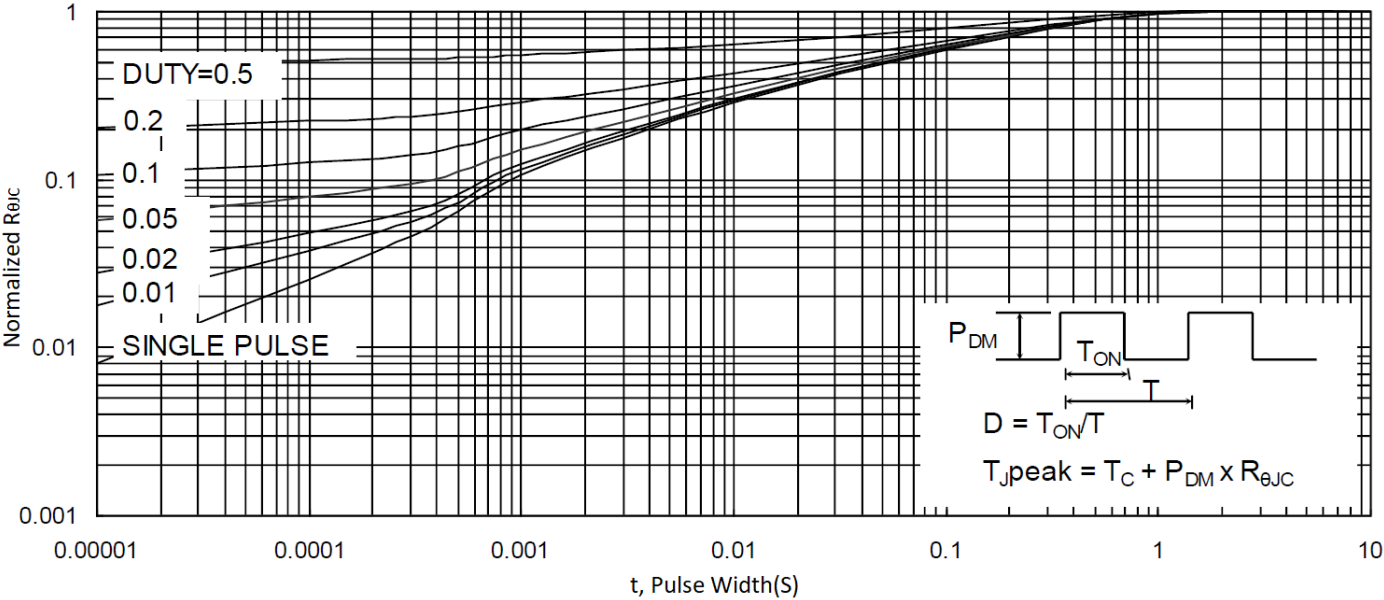


Figure 9. Normalized Maximum Transient Thermal Impedance

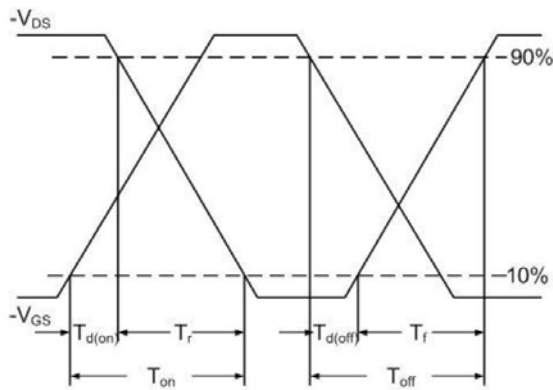


Figure 10. Switching Time Waveform

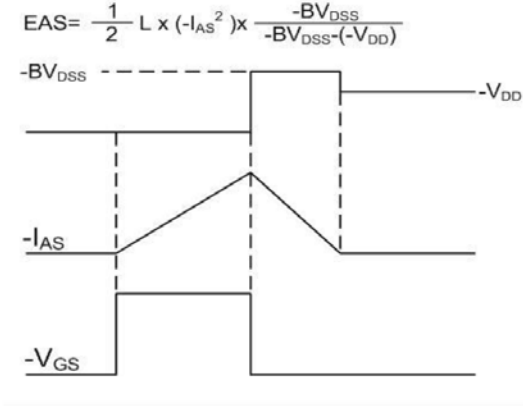


Figure 11. Unclamped Inductive Switching Waveform

Test Circuit

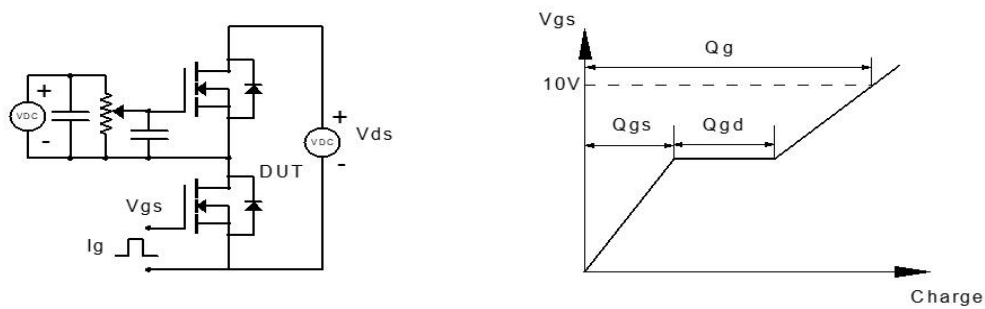


Figure 1: Gate Charge Test Circuit & Waveform

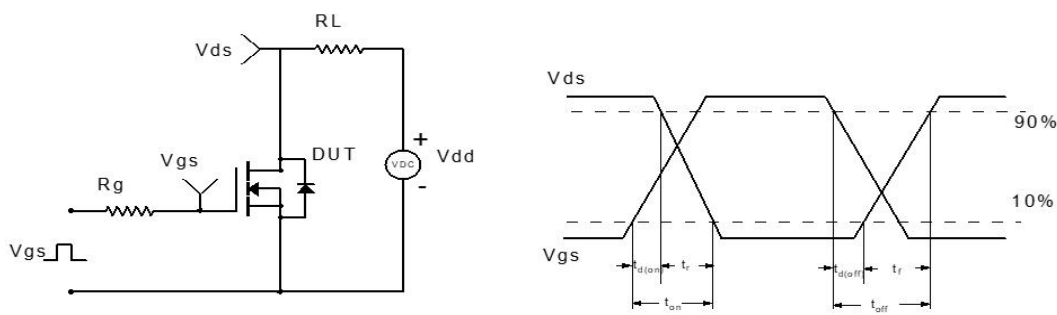


Figure 2: Resistive Switching Test Circuit & Waveform

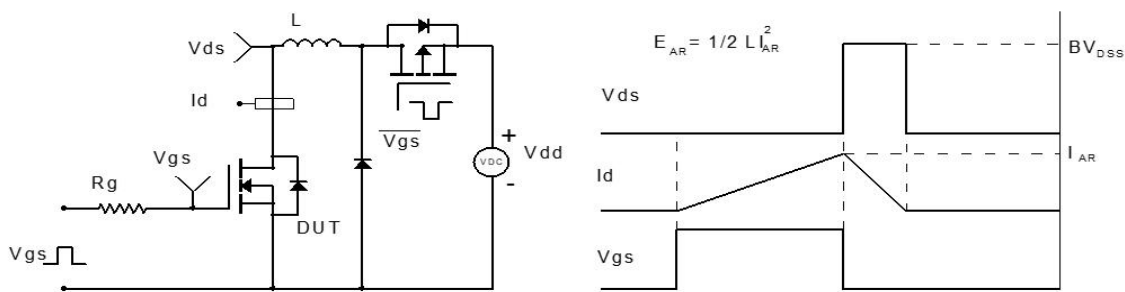


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

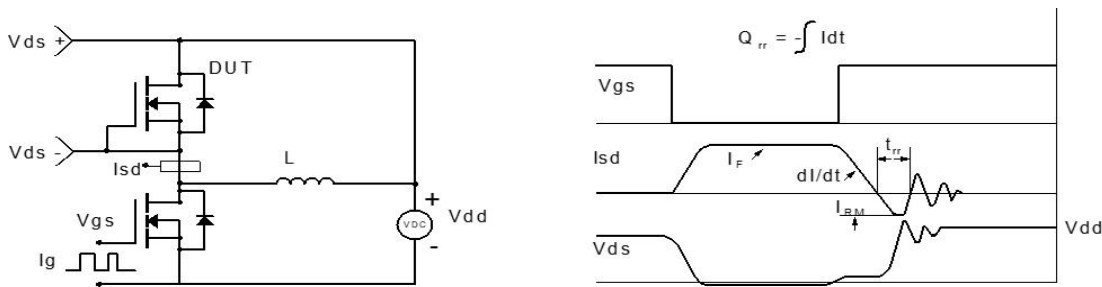
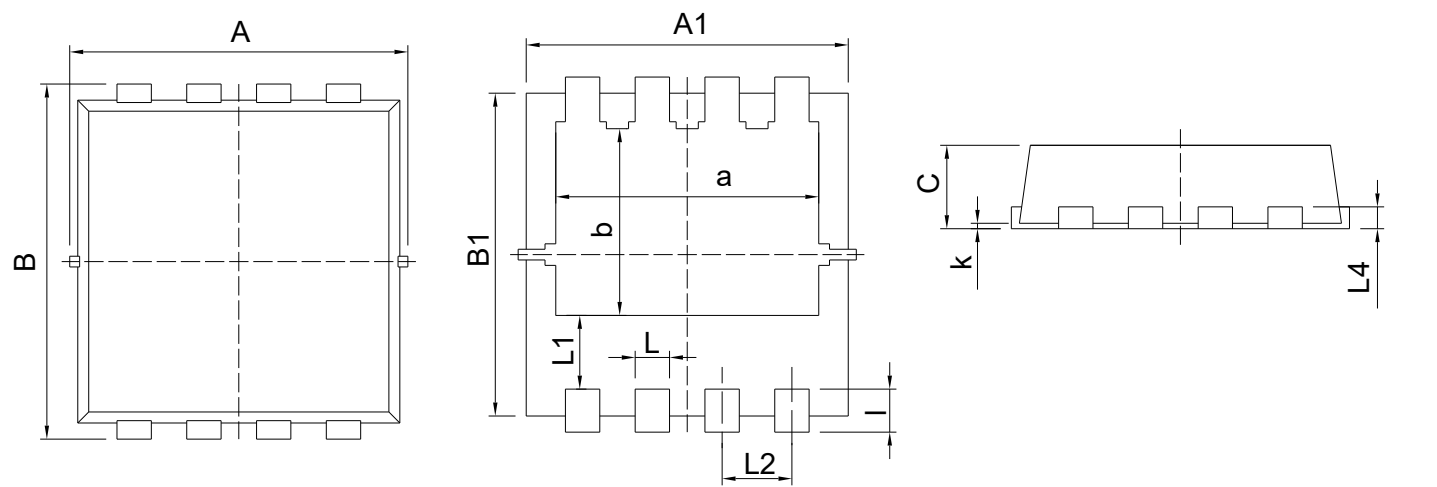


Figure 4: Diode Recovery Test Circuit & Waveform

Package Outline

PDFN3x3-8L Dimensions in mm

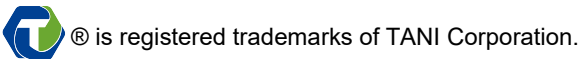


Symbol	Dimensions		Symbol	Dimensions	
	Min.	Max.		Min.	Max.
A	3.2	3.4	L2	0.55	0.75
A1	3.1	3.2	L4	0.14	0.20
B	3.2	3.4	a	2.35	2.55
B1	2.95	3.05	b	1.635	1.835
C	0.75	0.85	k	0.0	0.05
L	0.25	0.35	l	0.3	0.5
L1	-	0.75			

Contact Information

TANI website: <http://www.tanisemi.com> Email:tani@tanisemi.com

For additional information, please contact your local Sales Representative.



Product Specification Statement

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