

TN52 Series

Low Dropout Regulators

Description

TN52 series are the low noise LDO with enable function, the output operates from 0.8V to 5.0V by 0.1V/step. The characteristics are low noise and good PSRR and low dropout voltage, make this device ideal for portable consumer applications.

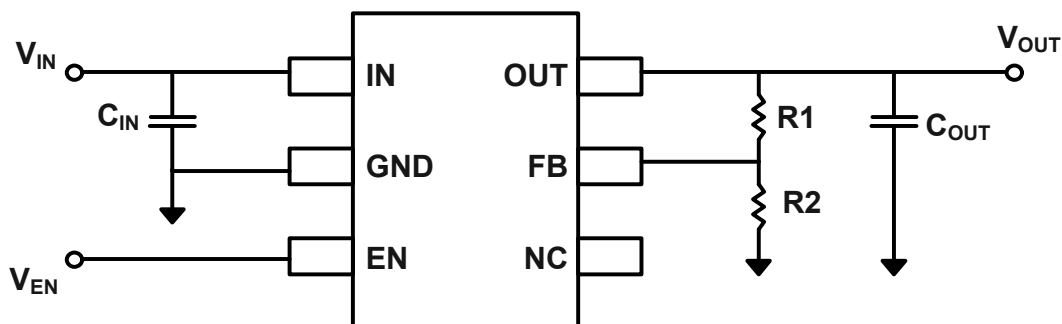
Features

- Wide Input Voltage Range: 2.7V~24V
- Maximum Output Current: 1A
- Standard Fixed Output Voltage Options: 0.8V~5.0V(customized by every 0.05V step)
Adjustable Output Voltages: $V_{FB}=0.6V$
- Quiescent Current: 160uA(Typ.)
- PSRR=80dB @ 1KHz
- Low Dropout Voltage: 600mV@1A($V_{out} \geq 2V$)
- Output Voltage Accuracy: $\pm 2\%$
- Available Packages: SOT-89, TO-252, ESOP-8, DFN2x2C-6L

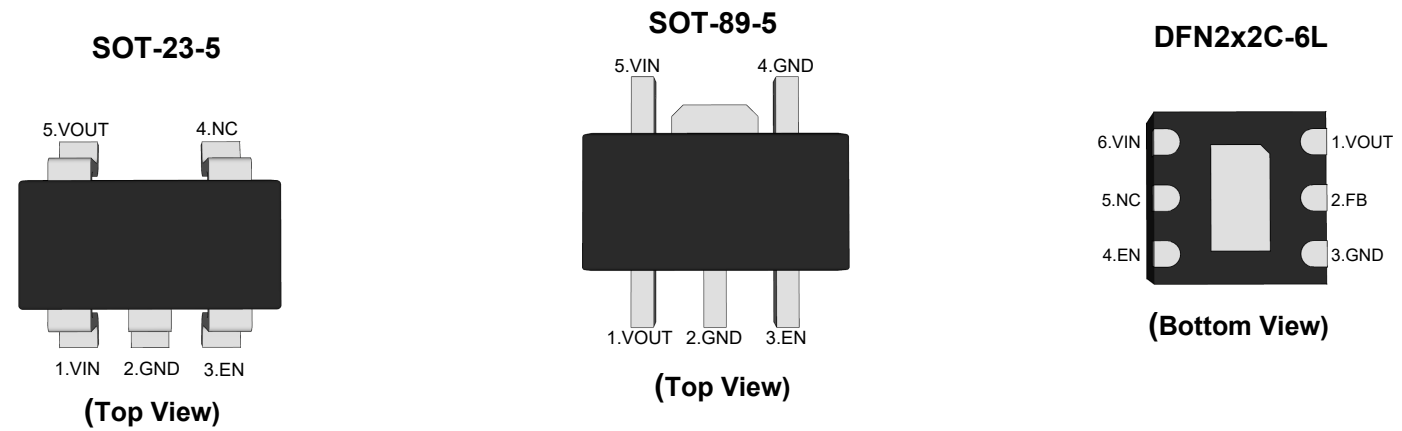
Applications

- Consumer and Industrial Equipment Point of Regulation
- Switching Power Supply Post Regulation
- Battery Chargers
- Hard Drive Controllers

Typical Application Circuit



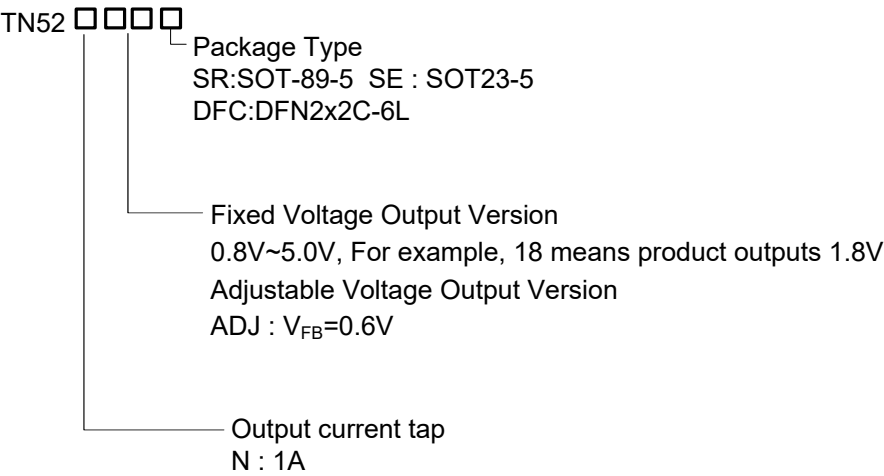
Pin Distribution



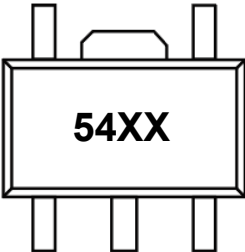
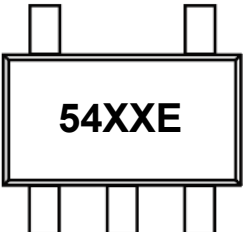
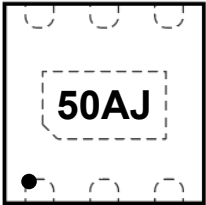
Functional Pin Description

Pin Name	Pin Function
VIN	Power Input Voltage
GND	Ground
VOUT	Output Voltage
EN	Chip Enable (Active High). Note that this pin is high impedance
NC	NO Connected
FB	Feedback Pin (adjustable voltage version only). Connect this pin to the midpoint of an external resistor divider to adjust the output voltage

Ordering Information



Ordering Information Continue

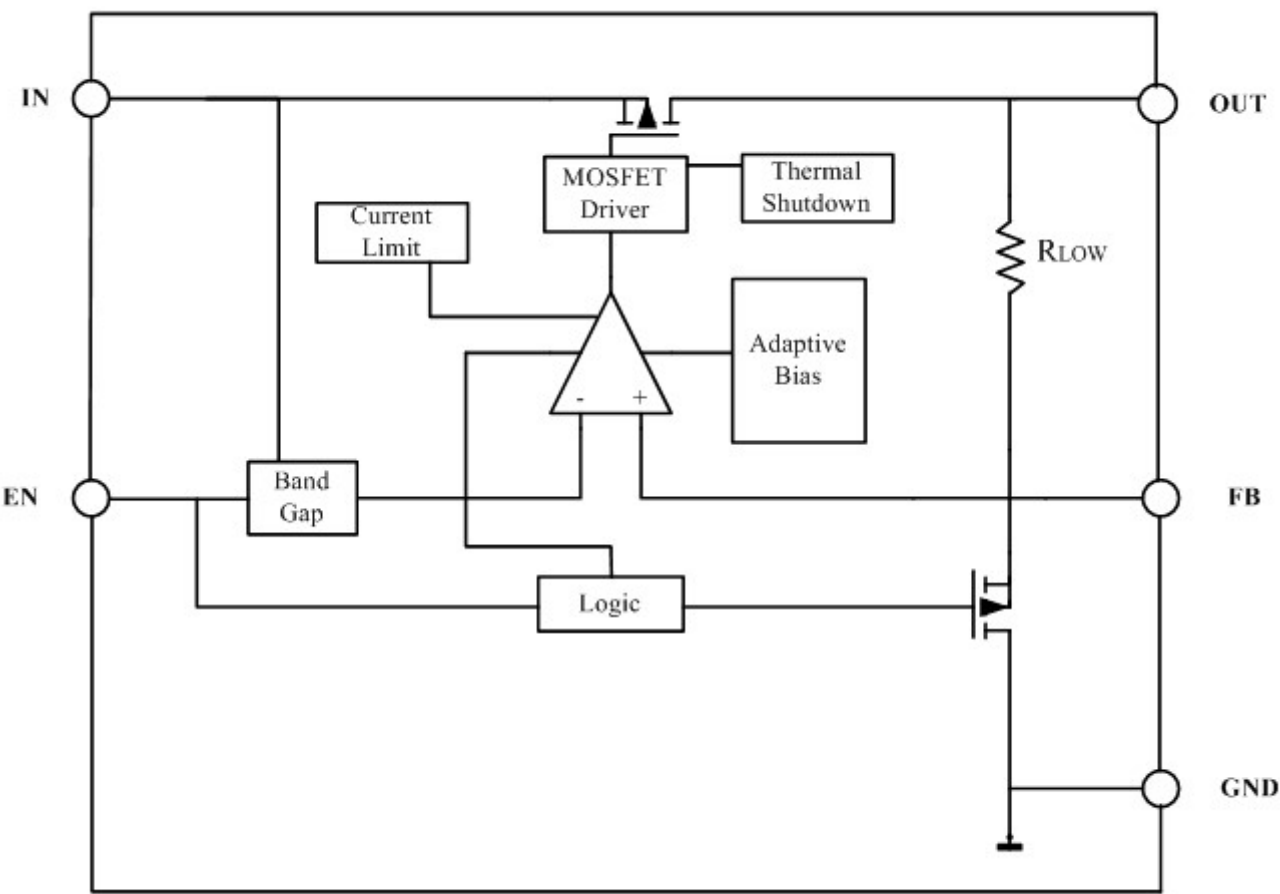
Orderable Device	Package	Reel (inch)	Package Qty (PCS)	Eco Plan ^{Note1}	MSL Level	Marking Code
TN52NXXSR ^{Note2}	SOT-89-5	7/13	1000/3000	RoHS & Green	MSL1	 XX: Output Voltage e.g. 18:1.8V
TN52NXXSE ^{Note2}	SOT-23-5	7	3000	RoHS & Green	MSL3	 XX: Output Voltage e.g. 18:1.8V
TN52NADJDFC	DFN2x2C-6L	7	3000	RoHS & Green	MSL1	

Note:

1. RoHS: TN defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials.
Green: TN defines "Green" to mean Halogen-Free and Antimony-Free.

2. XX indicates 0.8V~5.0V . For example, 18 means product outputs 1.8V.

Function Block Diagram



Absolute Maximum Ratings ^{Note1}

Ratings at 25°C ambient temperature unless otherwise specified.

Parameter		Value	Unit
Max Input Voltage ^{Note2}		0~24	V
Output Voltage		0.8~6	V
Chip Enable Input		-0.3~22	V
Power Dissipation	SOT-23-5	500	mW
	SOT-89-5	920	mW
	DFN2x2C-6L	1200	mW
	ESOP-8	800	mW
Thermal Resistance,Junction-to-Ambient	SOT-23-5	500	mW
	SOT-89-5	920	mW
	DFN2x2C-6L	80	°C/W
	ESOP-8	128	°C/W
Junction Temperature		150	°C
Storage Temperature Range		-55~ +150	°C
ESD Voltage ^{Note3}	HBM	2000	V
	CDM	1500	V
Current Maximum Rating		200	mA

Note:

1. Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect.
2. Refer to Electrial Characteristics and Application Information for Safe Operating Area.
3. This device series incorporates ESD protection and is tested by the following methods:
ESD Human Body Model tested per EIA/JESD22-A114
CDM tested per JESD22-C101 ; Latch up Current Maximum Rating tested per JEDEC78

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V _{IN}	2.7~22	V
Output Current	I _{OUT}	0~1	A
Operating Ambient Temperature	T _{OPR}	-40 ~ +85	°C
Input and Output Capacitor Equivalent Series Resistance	ESR	5 ~ 100	mΩ

Electrical Characteristics

$V_{IN}=V_{OUT}+1V$, $I_{OUT}=10mA$, $C_{IN}=10\mu F$, $C_{OUT}=10\mu F$, $T_A=25^{\circ}C$, unless otherwise noted.)

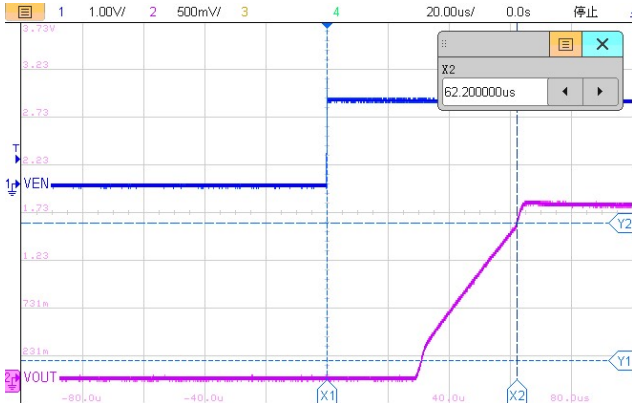
Parameter		Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Input Voltage		V _{IN}			2.7	--	20	V
Output Voltage Accuracy		ΔV _{OUT}	T _A =25°C		-2	--	+2	%
			T _A =-40°C ~ 85°C		-3	--	+3	%
Reference Voltage		V _{REF}			0.588	0.60	0.612	V
Quiescent Current		I _Q	I _{OUT} =0A		--	160	190	μA
Dropout Voltage		V _{DROP}	V _{OUT} =1.8V	I _{OUT} =1A, V _{IN} ≥ 2.7V, T _A =-40°C~125°C	--	750	800	mV
			V _{OUT} =3.3V		--	480	600	mV
			V _{OUT} =5.0V		--	450	550	mV
			V _{OUT} =1.8V	I _{OUT} =500mA, V _{IN} ≥2.7V, T _A =-40°C~125°C	--	650	900	mV
			V _{OUT} =3.3V		--	210	450	mV
			V _{OUT} =5.0V		--	200	400	mV
Line Regulation		ΔV _{LINE}	I _{OUT} =10mA, 2.8V ≤ V _{IN} ≤ 20V		--	0.05	0.2	%/V
Load Regulation		ΔV _{LOAD}	1mA≤ I _{OUT} ≤ 800mA, V _{IN} =V _{OUT} +1V		--	--	40	mV
Short Circuit/Start Carrying Current		I _{SHORT}	V _{OUT} = 0V		--	330	--	mA
Current Limit		I _{LIMIT}	V _{IN} =V _{OUT} +1V		1.04	1.3	--	A
Shutdown Current		I _{SHDN}	V _{EN} =0V		--	0.1	1	μA
Power Supply Rejection Ratio		PSRR	V _{IN} =V _{OUT} +2V I _{OUT} =50mA	f=1 KHz	--	80	--	dB
				f=100 KHz	--	70	--	dB
				f=1M KHz	--	65	--	dB
EN Input Threshold	Logic Low	V _{ENL}	EN Low Voltage		--	--	0.4	V
	Logic High	V _{ENH}	EN High Voltage		1.4	--	--	V
EN Pin Current		I _{EN}	V _{EN} ≤ V _{IN} ≤ 20V		--	1	--	μA
Output Noise Voltage		eN	V _{IN} = V _{OUT} +1V, I _{OUT} = 1mA, f=10Hz to100KHz, (V _{OUT} =3V), C _{OUT} =1μF		--	30*V _{OUT}	--	μV _{RMS}
Thermal Shut down Temperature		T _{SD}	Temperature Increasing from T _A =25°C		--	150	--	°C
Thermal Shutdown Hysteresis		T _{SDH}	Temperature Falling from T _{SD}		--	25	--	°C

Typical Electrical Curves

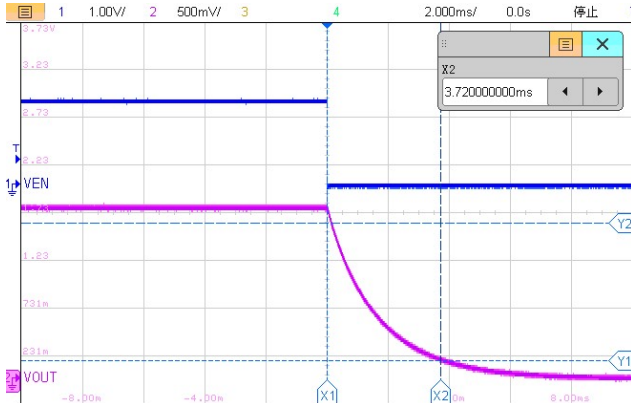
Test conditions: $V_{IN}=V_{OUT}+1V$, $I_{OUT}=1mA$, C_{IN} =Ceramic $10\mu F$, C_{OUT} =Ceramic $10\mu F$ (unless otherwise noted)

T_{ON} and T_{OFF}

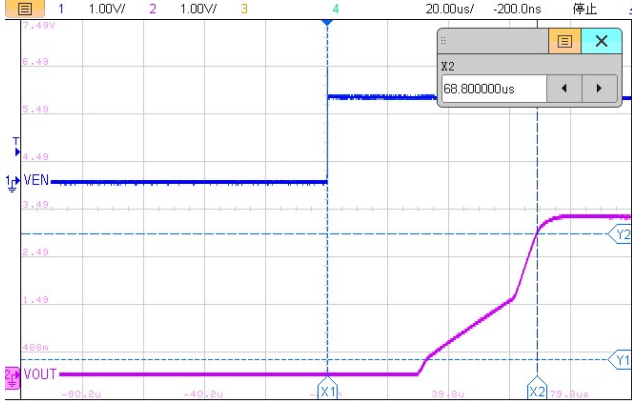
Turn On VS EN Voltage ($V_{OUT}=1.8V$, $I_{OUT}=0mA$)



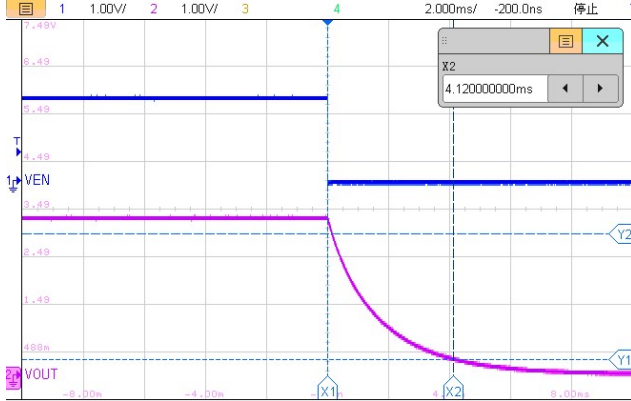
Turn Off VS EN Voltage ($V_{OUT}=1.8V$, $I_{OUT}=0mA$)



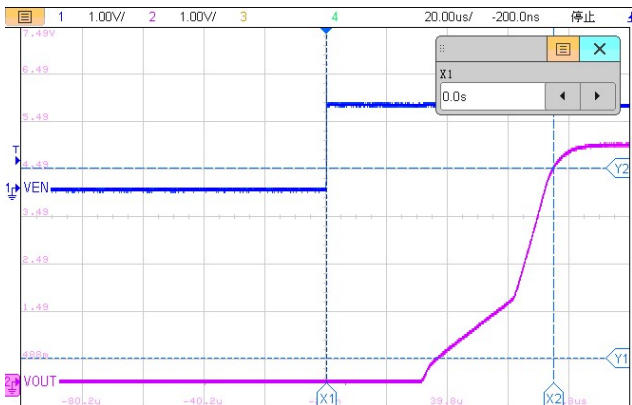
Turn On VS EN Voltage ($V_{OUT}=3.3V$, $I_{OUT}=0mA$)



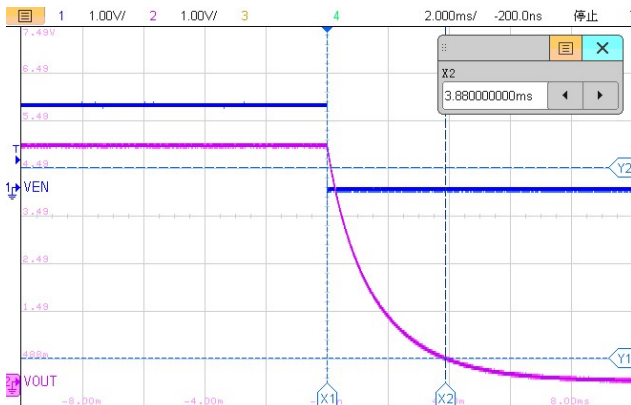
Turn Off VS EN Voltage ($V_{OUT}=3.3V$, $I_{OUT}=0mA$)



Turn On VS EN Voltage ($V_{OUT}=5.0V$, $I_{OUT}=0mA$)

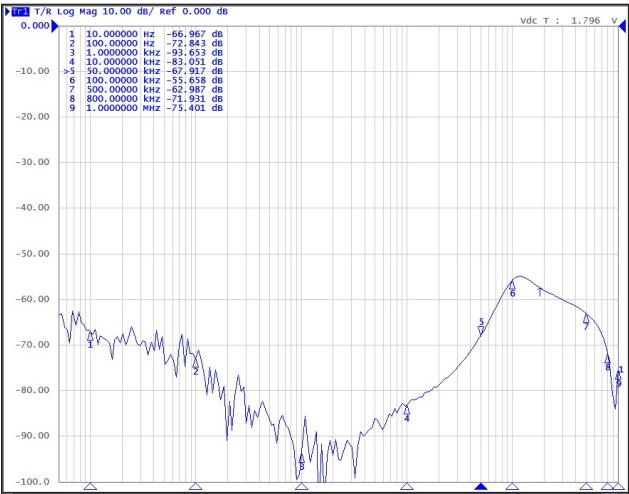


Turn Off VS EN Voltage ($V_{OUT}=5.0V$, $I_{OUT}=0mA$)

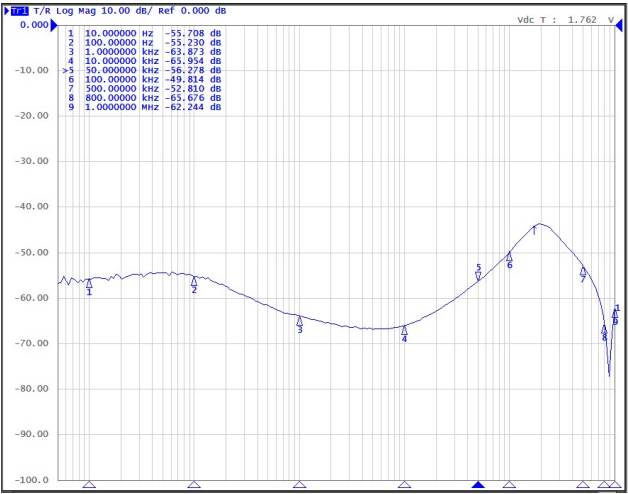


PSRR

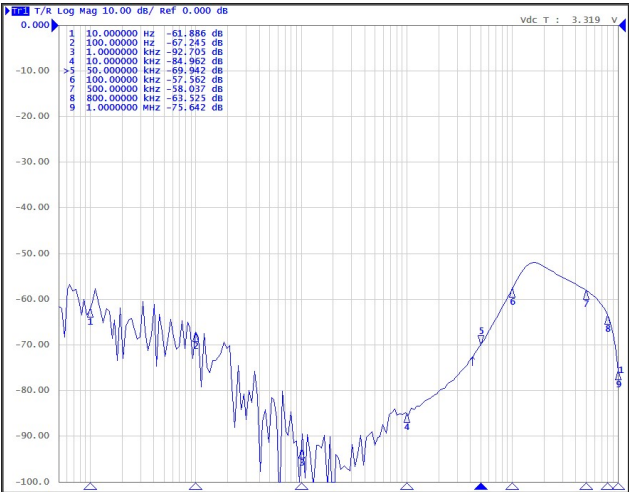
PSRR VS I_{OUT}(V_{OUT}=1.8V, I_{OUT}=50mA)



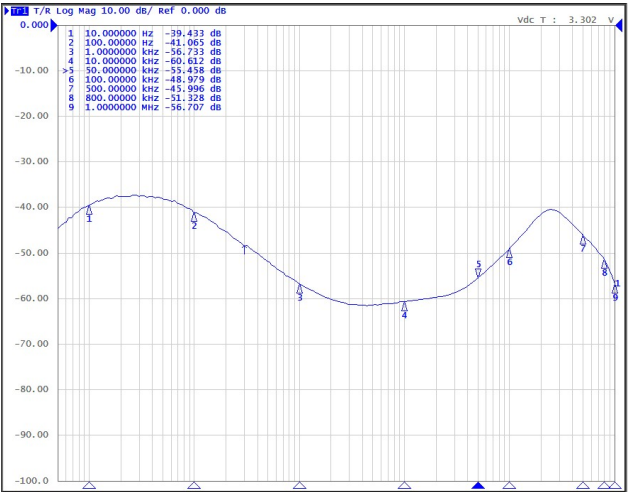
PSRR VS I_{OUT}(V_{OUT}=1.8V, I_{OUT}=500mA)



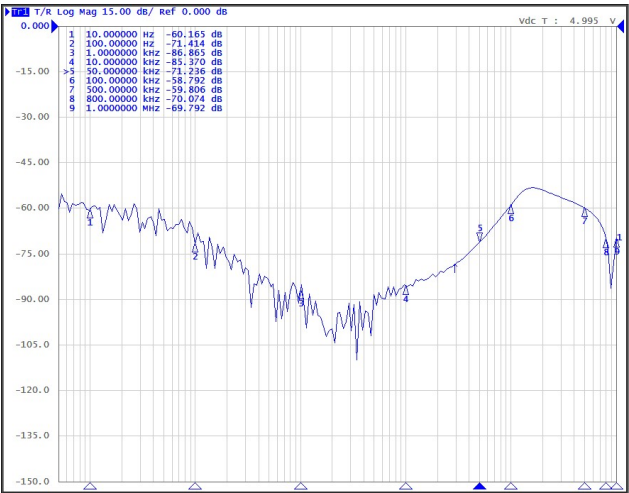
PSRR VS I_{OUT}(V_{OUT}=3.3V, I_{OUT}=50mA)



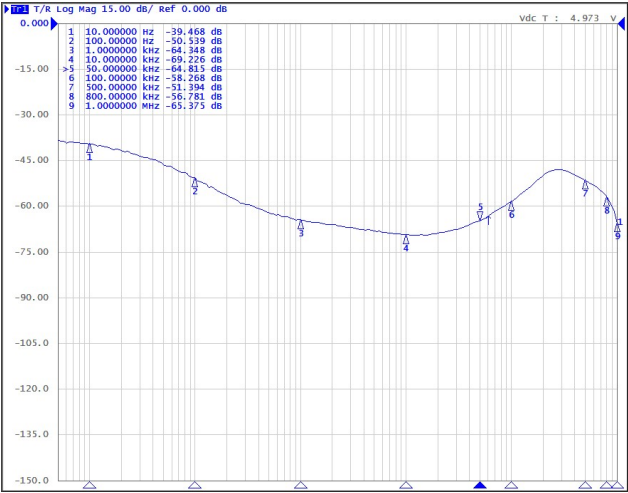
PSRR VS I_{OUT}(V_{OUT}=3.3V, I_{OUT}=500mA)



PSRR VS I_{OUT}(V_{OUT}=5.0V, I_{OUT}=50mA)

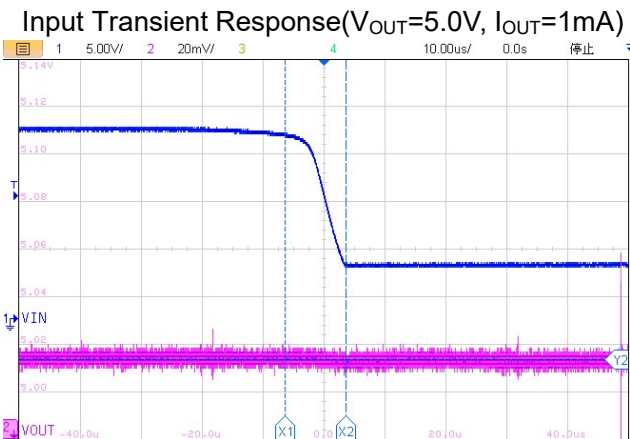
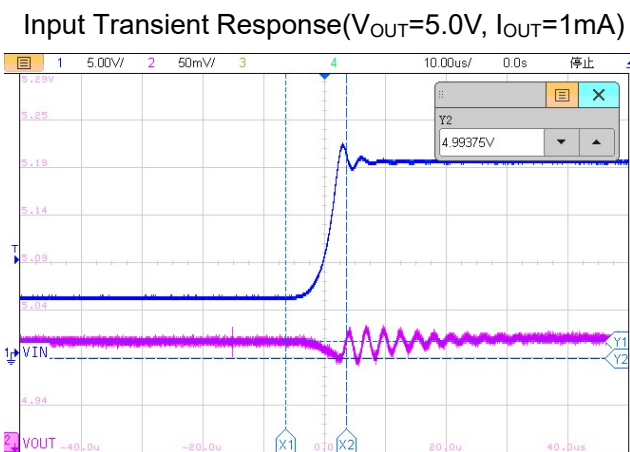
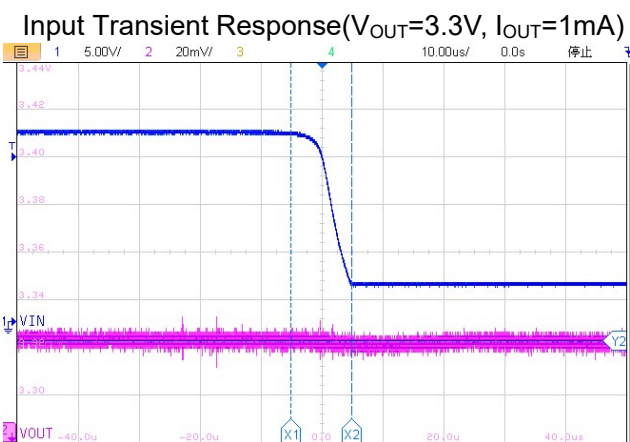
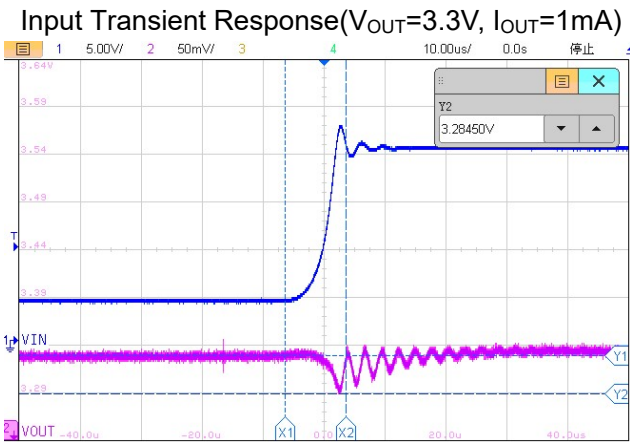
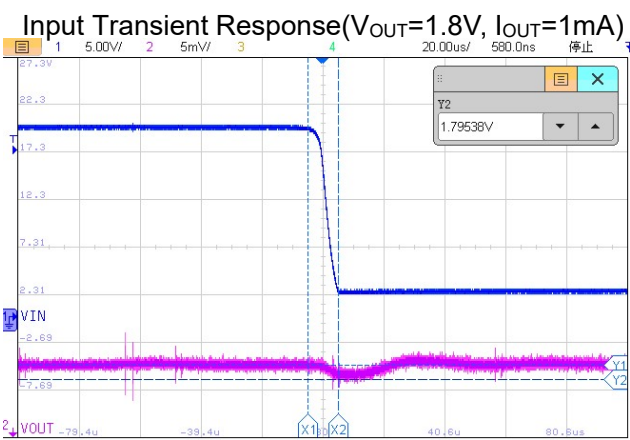
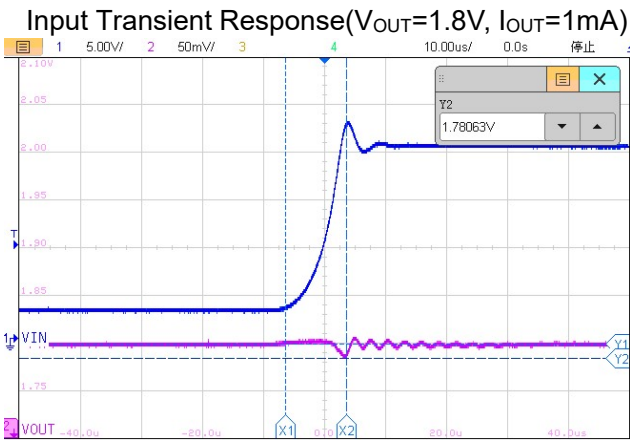


PSRR VS I_{OUT}(V_{OUT}=5.0V, I_{OUT}=500mA)



Input Transient Response

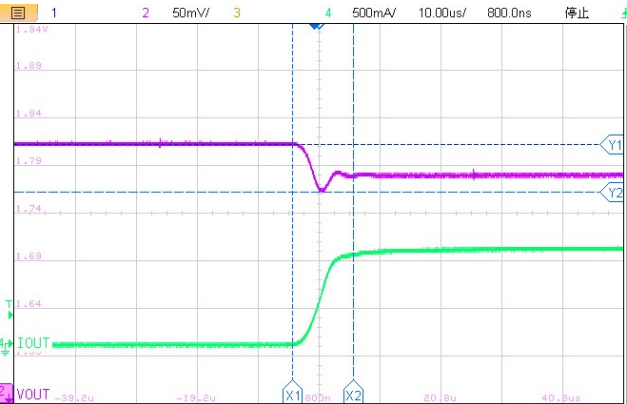
Test conditions: $V_{IN}=V_{OUT}+1V$, $I_{OUT}=10mA$, $t=10\mu S$, $C_{OUT}=10\mu F$, V_{IN} jump from 6V to 18V



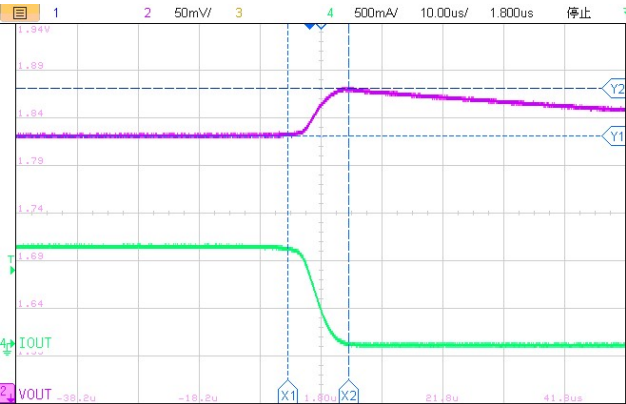
Load Transient Response

Test conditions: $V_{IN}=V_{OUT}+1V$, $t=10\mu S$, I_{OUT} jump from 1mA to 1000mA

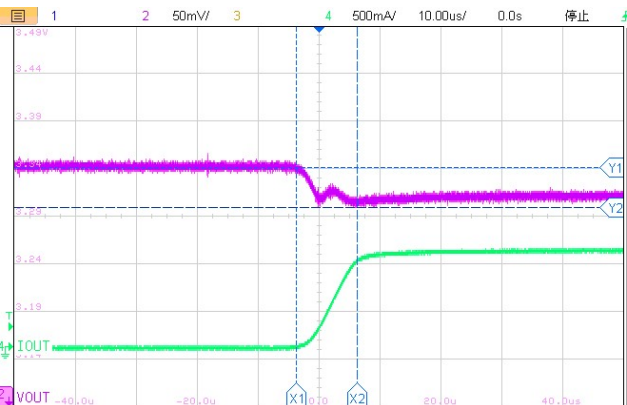
Load Transient Response($V_{OUT}=1.8V, I_{OUT}=1\sim1000mA$)



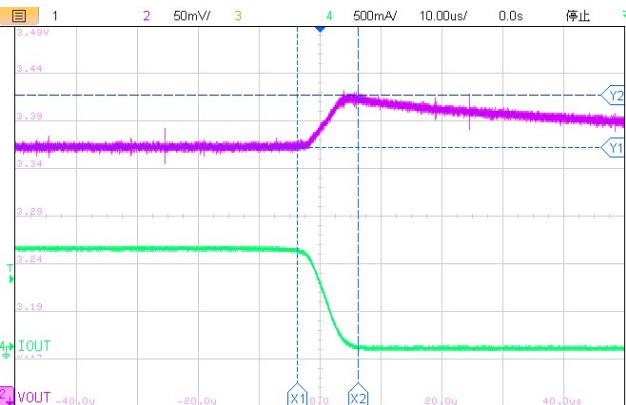
Load Transient Response($V_{OUT}=1.8V, I_{OUT}=1\sim1000mA$)



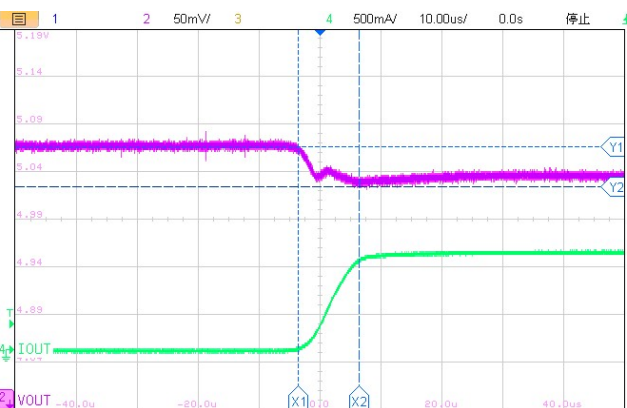
Load Transient Response($V_{OUT}=3.3V, I_{OUT}=1\sim1000mA$)



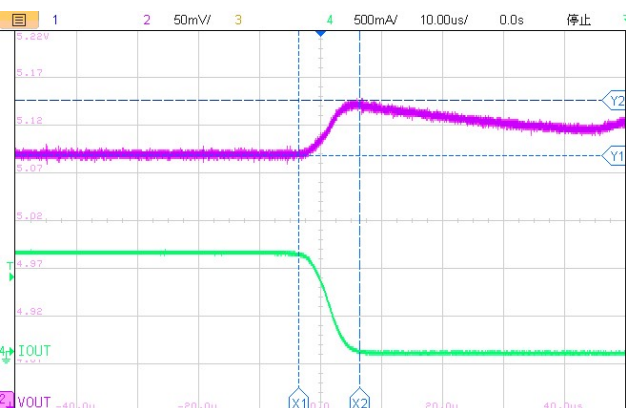
Load Transient Response($V_{OUT}=3.3V, I_{OUT}=1\sim1000mA$)



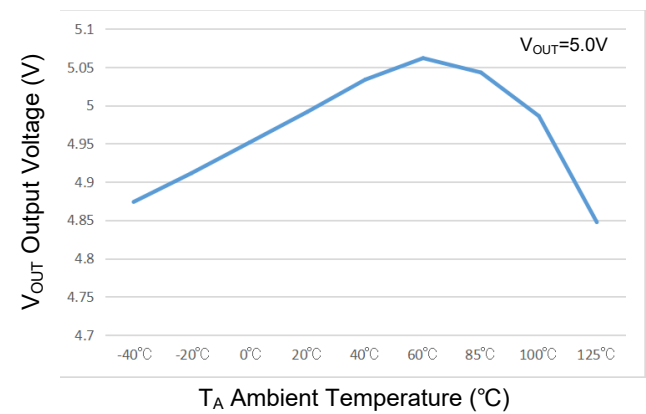
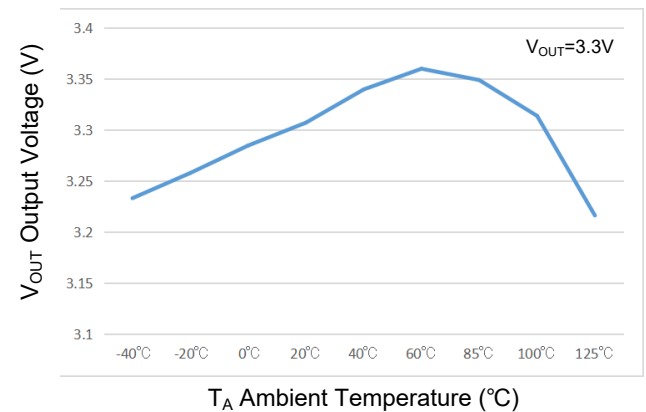
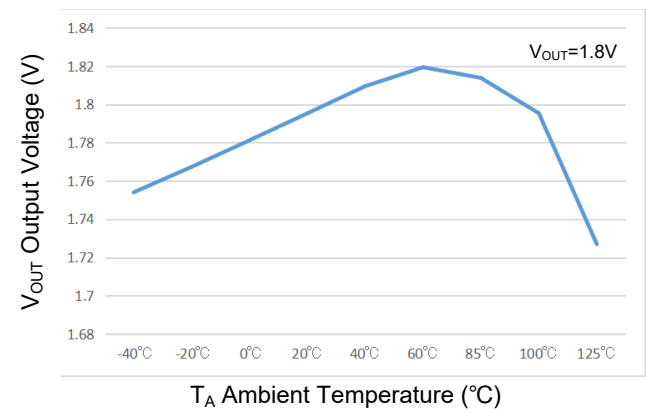
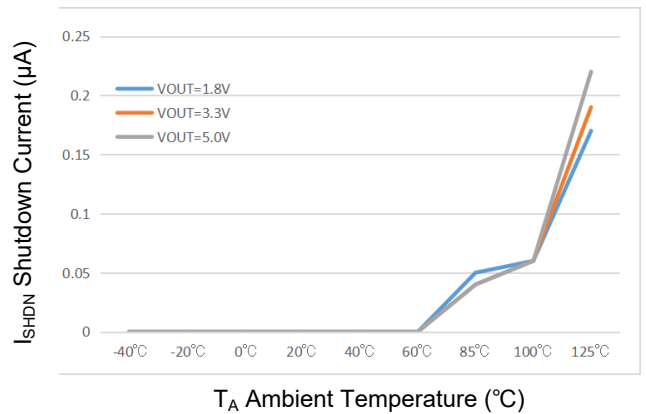
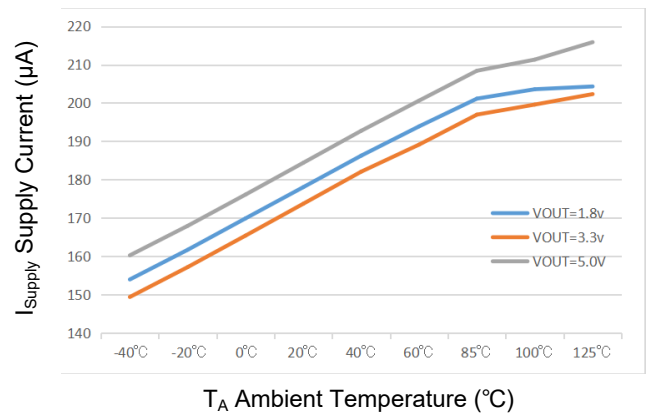
Load Transient Response($V_{OUT}=5.0V, I_{OUT}=1\sim1000mA$)



Load Transient Response($V_{OUT}=5.0V, I_{OUT}=1\sim1000mA$)



Temperature Characteristics



Application Information

Capacitor Selection

The TN52 Series requires an output capacitance of 4.7μF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application, pay attention to the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improve transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

Application of Electrolytic Capacitor

If the electrolytic capacitor should be used as input and output capacitor, the capacitance of the capacitor must be greater. The capacity value must be greater than 22μF.

Enable

The TN52 Series has an EN pin to turn on or turn off the regulator. When the EN pin is in logic high, the regulator will be turned on. The shutdown current is almost 0μA typical. The EN pin may be directly tied to V_{IN} to keep the part on. The Enable input is CMOS logic and cannot be left floating.

Setting the Output Voltage

The TN52 Series develops a 0.6V reference voltage, V_{REF}, between the output and the adjust terminal. This voltage is applied across resistor R1 to generate a constant current. The current I_{ADJ} from the ADJ terminal could introduce DC offset to the output. Because, this offset is very small (about 0.1 μA), it can be ignored. The constant current then flows through the output set resistor R2 and sets the output voltage to the desired level. Equation 2 is used for calculating V_{OUT}:

$$V_{OUT} = 0.6V \times (1 + R1 / R2)$$

Although I_{ADJ} is very small, R1+R2 should be limited to less than 100 KΩ for optimum performance.

Dropout Voltage

The TN52 Series uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the R_{DS(ON)} of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation.

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 150°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 125°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$$

Where $T_{J(MAX)}$ is the maximum junction temperature of the die (150°C), T_A is the maximum ambient temperature, and $R_{\theta JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, $R_{\theta JA}$, is layout dependent. For DFN2x2C-6L package, the thermal resistance, $R_{\theta JA}$, is 80°C/W on the test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by the following formula:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (80^\circ\text{C/W}) = 1.25\text{W for DFN2x2C-6L package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $R_{\theta JA}$. in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

Layout

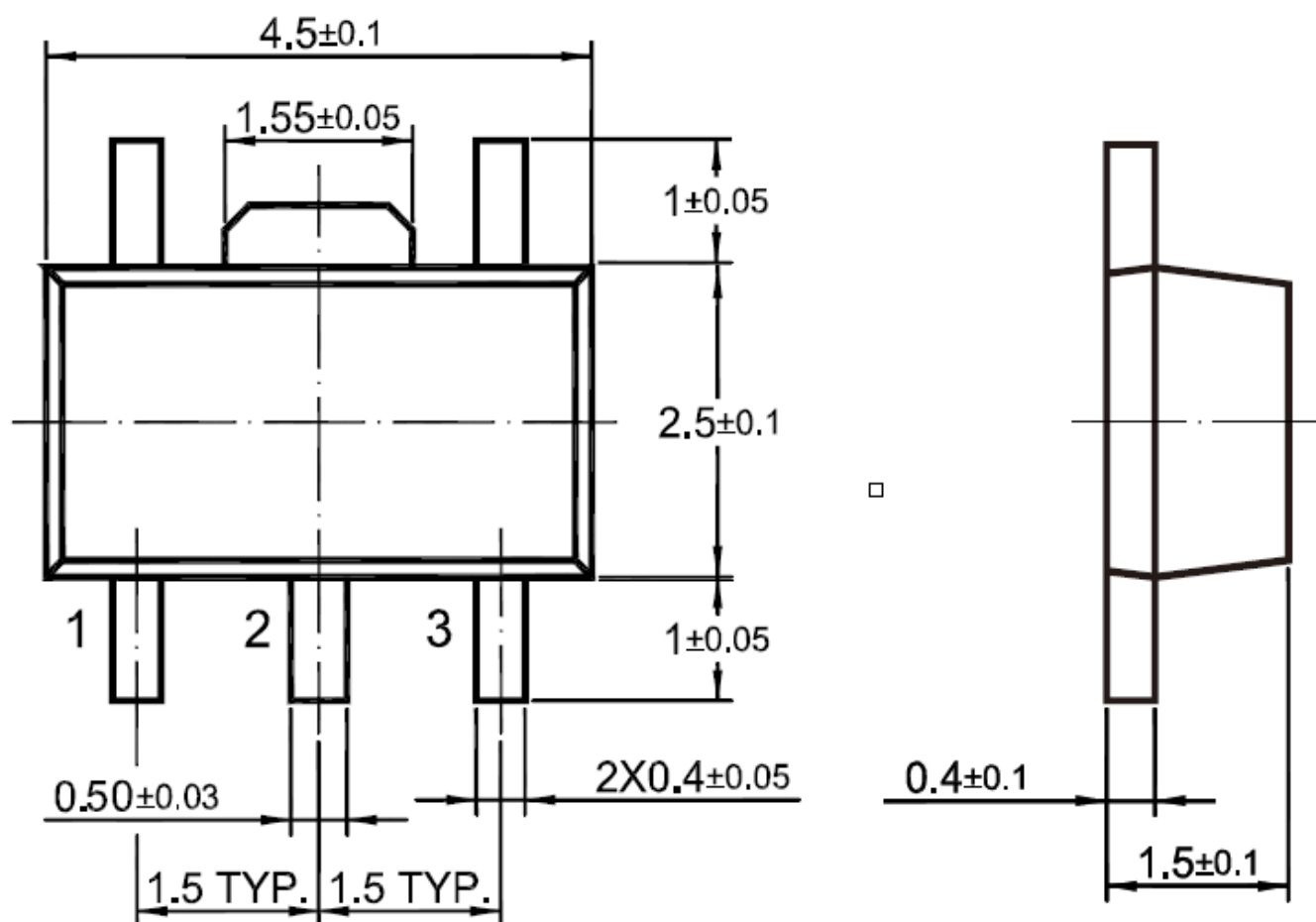
Layout Guidelines

1. Place input and output capacitors as close to the device as possible.
2. Use copper planes for device connections in order to optimize thermal performance.
3. Place thermal vias around the device to distribute heat.
4. Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

Package Outline

SOT-89-5

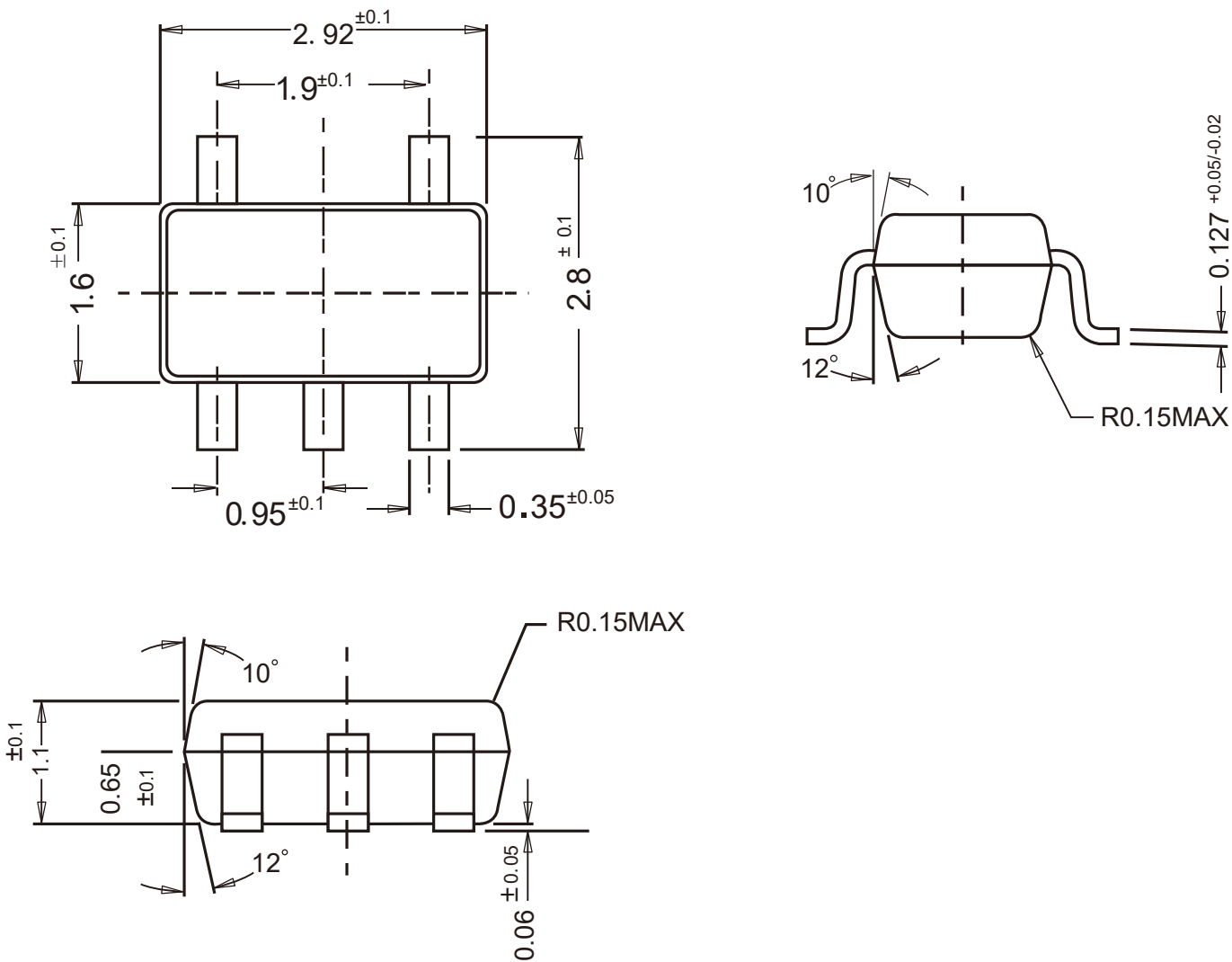
Dimensions in mm



Package Outline

SOT-23-5

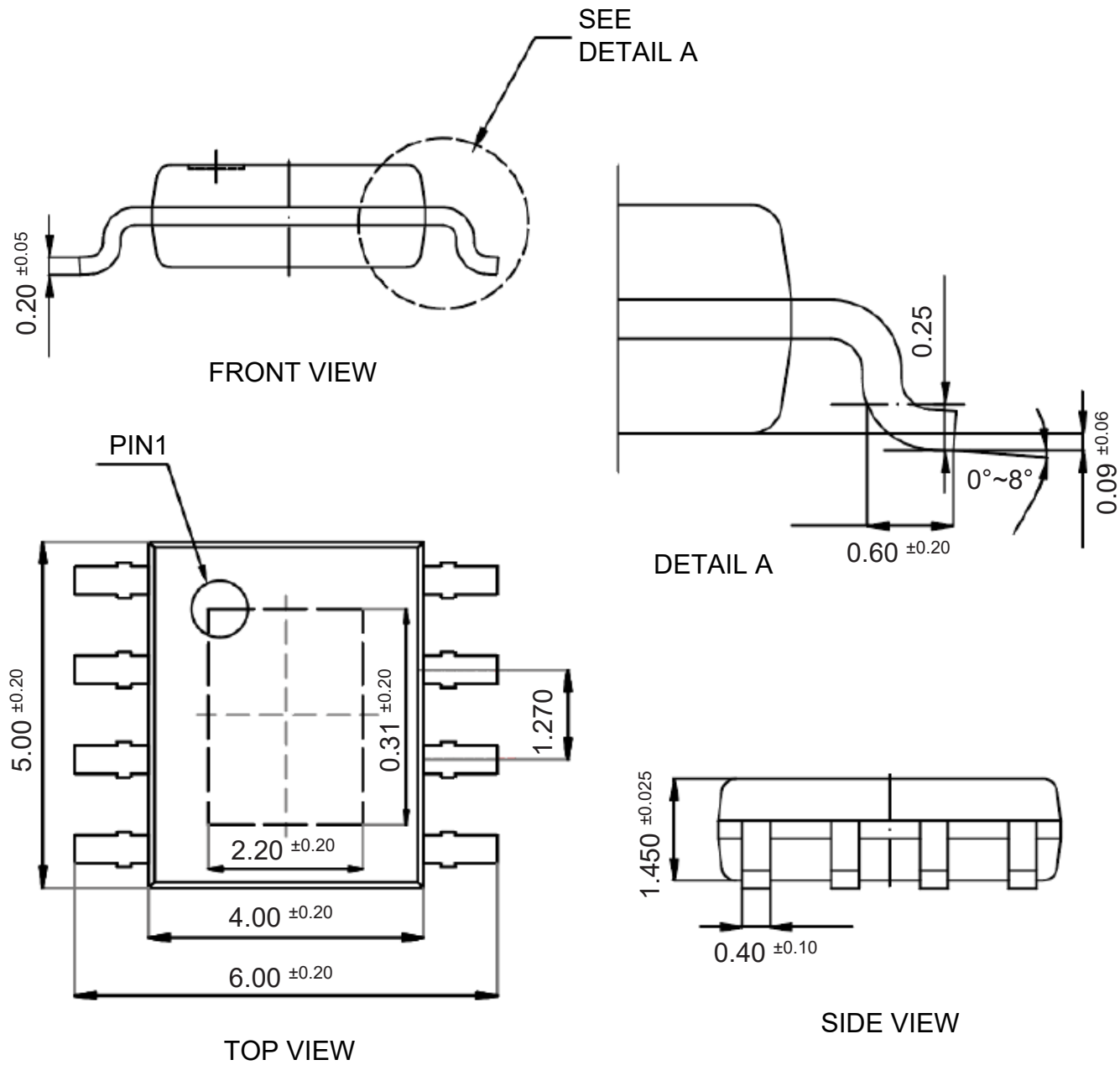
Dimensions in mm



Package Outline

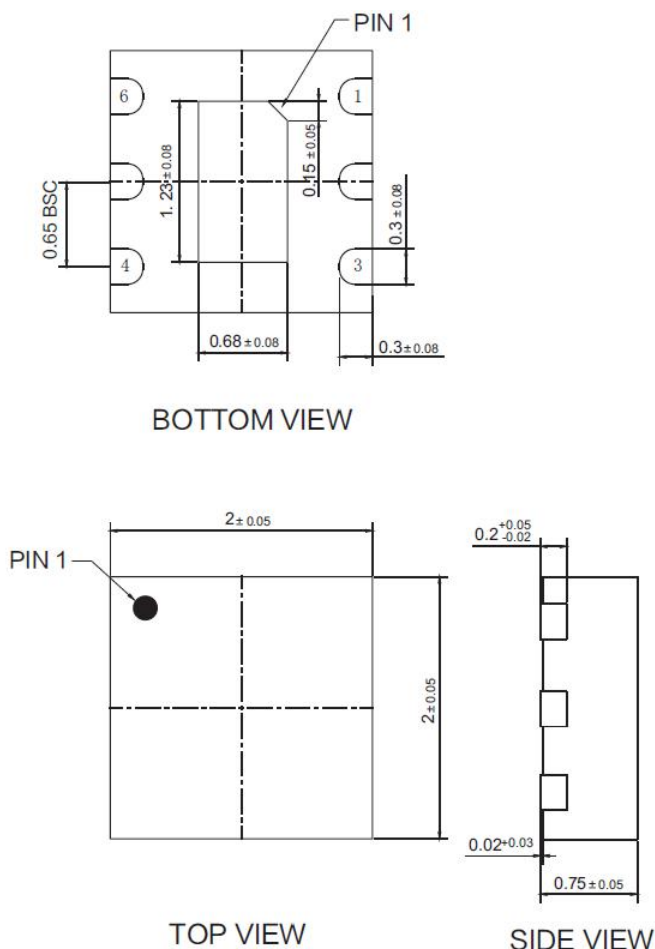
ESOP-8

Dimensions in mm



Package Outline

DFN2x2C-6L Dimensions in mm



Contact Information

TANI website: <http://www.tanisemi.com> Email: tani@tanisemi.com

For additional information, please contact your local Sales Representative.

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Product Specification Statement

The product specification aims to provide users with a reference regarding various product parameters, performance, and usage. It presents certain aspects of the product's performance in graphical form and is intended solely for users to select product and make product comparisons, enabling users to better understand and evaluate the characteristics and advantages of the product. It does not constitute any commitment, warranty, or guarantee.

The product parameters described in the product specification are numerical values, characteristics, and functions obtained through actual testing or theoretical calculations of the product in an independent or ideal state. Due to the complexity of product applications and variations in test conditions and equipment, there may be slight fluctuations in parameter test values. TANI shall not guarantee that the actual performance of the product when installed in the customer's system or equipment will be entirely consistent with the product specification, especially concerning dynamic parameters. It is recommended that users consult with professionals for product selection and system design. Users should also thoroughly validate and assess whether the actual parameters and performance when installed in their respective systems or equipment meet their requirements or expectations. Additionally, users should exercise caution in verifying product compatibility issues, and TANI assumes no responsibility for the application of the product. TANI strives to provide accurate and up-to-date information to the best of our ability. However, due to technical, human, or other reasons, TANI cannot guarantee that the information provided in the product specification is entirely accurate and error-free. TANI shall not be held responsible for any losses or damages resulting from the use or reliance on any information in these product specifications.

TANI reserves the right to revise or update the product specification and the products at any time without prior notice, and the user's continued use of the product specification is considered an acceptance of these revisions and updates. Prior to purchasing and using the product, users should verify the above information with TANI to ensure that the product specification is the most current, effective, and complete. If users are particularly concerned about product parameters, please consult TANI in detail or request relevant product test reports. Any data not explicitly mentioned in the product specification shall be subject to separate agreement.

Users are advised to pay attention to the parameter limit values specified in the product specification and maintain a certain margin in design or application to ensure that the product does not exceed the parameter limit values defined in the product specification. This precaution should be taken to avoid exceeding one or more of the limit values, which may result in permanent irreversible damage to the product, ultimately affecting the quality and reliability of the system or equipment.

The design of the product is intended to meet civilian needs and is not guaranteed for use in harsh environments or precision equipment. It is not recommended for use in systems or equipment such as medical devices, aircraft, nuclear power, and similar systems, where failures in these systems or equipment could reasonably be expected to result in personal injury. TANI shall assume no responsibility for any consequences resulting from such usage.

Users should also comply with relevant laws, regulations, policies, and standards when using the product specification. Users are responsible for the risks and liabilities arising from the use of the product specification and must ensure that it is not used for illegal purposes. Additionally, users should respect the intellectual property rights related to the product specification and refrain from infringing upon any third-party legal rights. TANI shall assume no responsibility for any disputes or controversies arising from the above-mentioned issues in any form.