TN51 Series

Low Dropout Regulators

Description

TN51 series are the low noise LDO with enable function, the output operates from 0.8V to 5.0V by 0.1V/ step. The characteristics are low noise and good PSRR and low dropout voltage, make this device ideal for portable consumer applications.

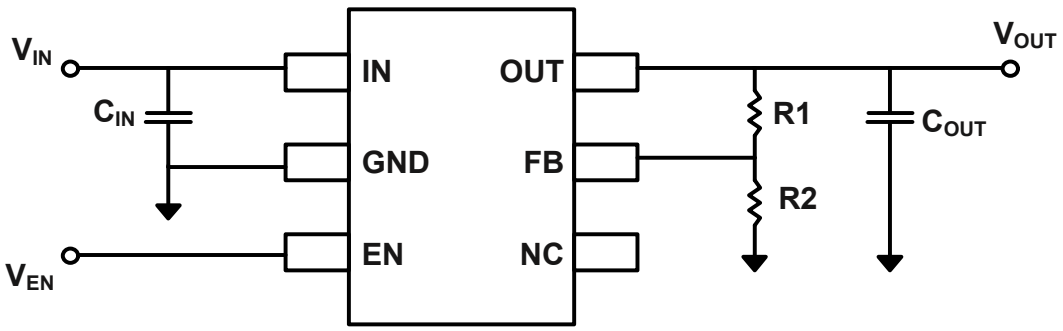
Features

- Wide Input Voltage Range: 2.7V~18V
- Maximum Output Current: 0.5A
- Standard Fixed Output Voltage Options: 0.8V~5.0V(customized by every 0.05V step)
  Adjustable Output Voltages: VFB=0.6V
- Quiescent Current: 160uA(Typ.)
- PSRR=80dB @ 1KHz
- Low Dropout Voltage: 600mV@0.5A(Vout≥2V)
- Output Voltage Accuracy: ±2%
- Available Packages: SOT-89, SOT23-3, SOT23-5

Applications

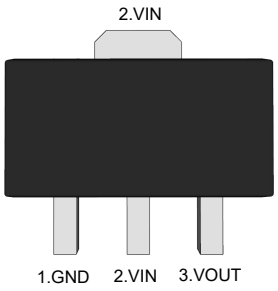
- Consumer and Industrial Equipment Point of Regulation
- Switching Power Supply Post Regulation
- Battery Chargers
- Hard Drive Controllers

Typical Application Circuit



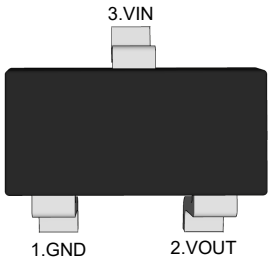
Pin Distribution

SOT-89



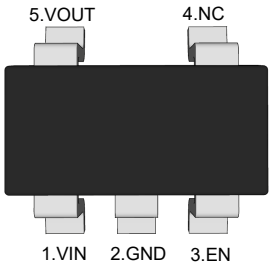
(Top View)

SOT-23-3



(Top View)

SOT-23-5



(Top View)

Functional Pin Description

Pin Name	Pin Function
VIN	Power Input Voltage
GND	Ground
VOUT	Output Voltage
EN	Chip Enable (Active High). Note that this pin is high impedance
NC	NO Connected
FB	Feedback Pin (adjustable voltage version only). Connect this pin to the midpoint of an external resistor divider to adjust the output voltage

Ordering Information

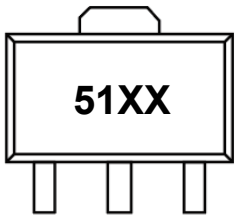
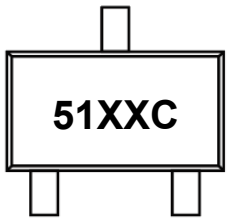
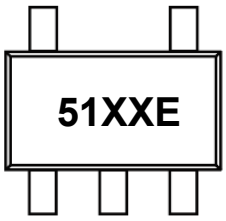
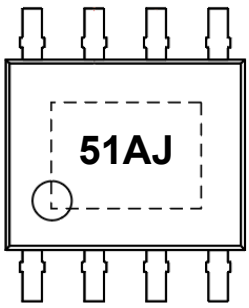
TN51 □□□□

Package Type
SQ : SOT-89 SC : SOT23-3
SE : SOT23-5

Fixed Voltage Output Version
0.8V~5.0V, For example, 18 means product outputs 1.8V
Adjustable Voltage Output Version
ADJ : V_{FB}=0.6V

Output current tap
N : 1A

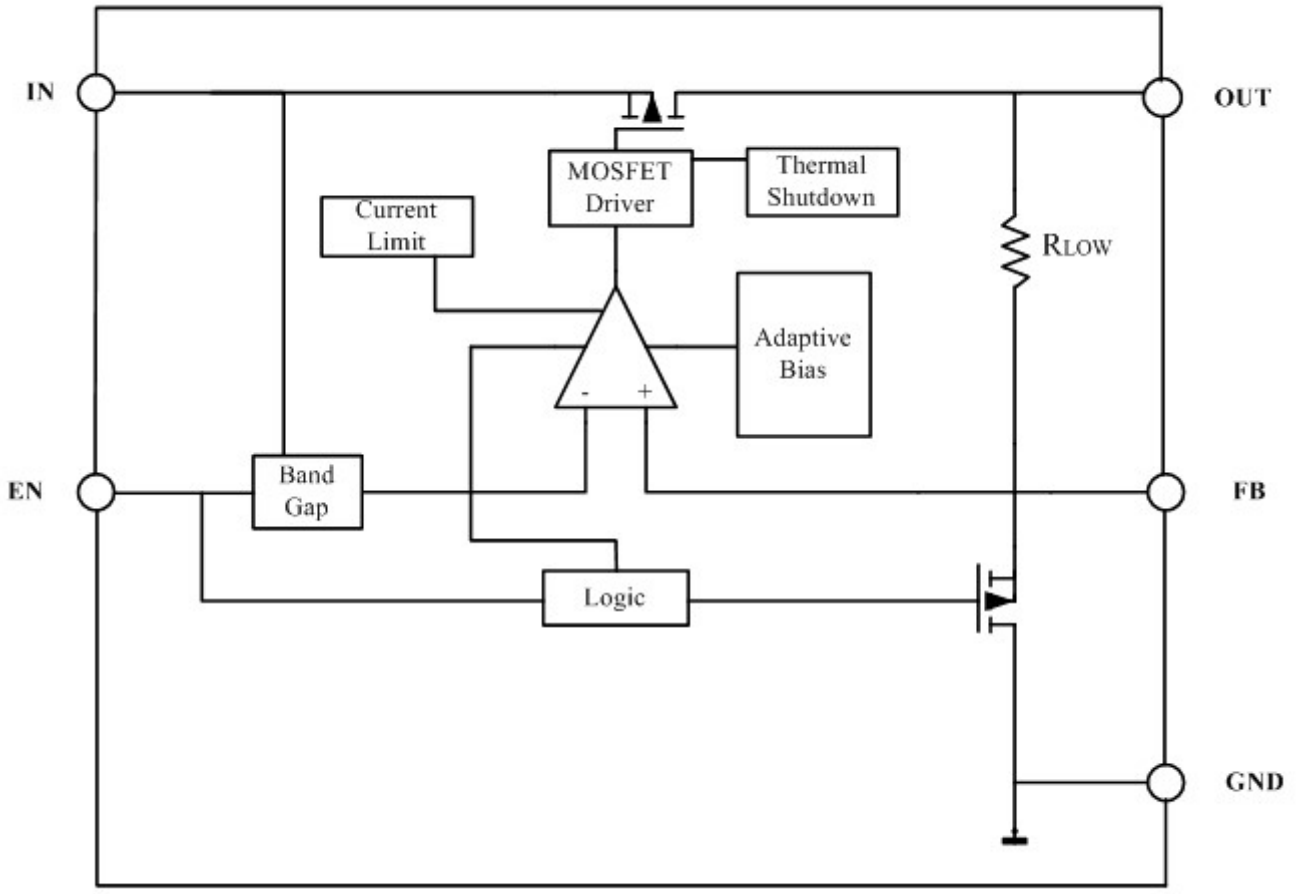
Ordering Information Continue

Orderable Device	Package	Reel (inch)	Package Qty (PCS)	Eco Plan Note1	MSL Level	Marking Code
TN51NXXSQ Note2	SOT-89	7/13	1000/3000	RoHS & Green	MSL1	 XX:Output Voltage e.g. 18:1.8V
TN51NXXSC Note2	SOT-23-3	7	3000	RoHS & Green	MSL3	 XX:Output Voltage e.g. 18:1.8V
TN51NADJSE	SOT-23-5	7	3000	RoHS & Green	MSL3	 XX:Output Voltage e.g. 18:1.8V
TN51NADJPB	ESOP-8	7	3000	RoHS & Green	MSL3	

Note:

1. RoHS: TN defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials.
   Green: TN defines "Green" to mean Halogen-Free and Antimony-Free.
2. XX indicates 0.8V~5.0V . For example, 18 means product outputs 1.8V.

Function Block Diagram



Absolute Maximum Ratings Note1

Ratings at 25℃ ambient temperature unless otherwise specified.

Parameter		Value	Unit
Max Input Voltage Note2		0~18	V
Output Voltage		0.8~5	V
Chip Enable Input		-0.3~22	V
Power Dissipation	SOT-89	500	mW
	SOT-23-3	500	mW
	SOT-23-5	500	mW
	ESOP-8	800	mW
Thermal Resistance,Junction-to-Ambient	SOT-89	200	°C/W
	SOT-23-3	500	mW
	SOT-23-5	500	mW
	ESOP-8	128	°C/W
Junction Temperature		150	°C
Storage Temperature Range		-55~ +150	°C
ESD Voltage Note3	HBM	2000	V
	CDM	1500	V
Current Maximum Rating		200	mA

Note:

1. Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect.
2. Refer to Electrial Characteristics and Application Information for Safe Operating Area.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22-A114
   CDM tested per JESD22-C101 ; Latch up Current Maximum Rating tested per JEDEC78

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{IN}	2.7~22	V
Output Current	I_{OUT}	0~1	A
Operating Ambient Temperature	T_{OPR}	-40 ~ +85	°C
Input and Output Capacitor Equivalent Series Resistance	ESR	5 ~ 100	mΩ

Electrical Characteristics

(V_{IN}=V_{OUT}+1V, I_{OUT}=10mA, C_{IN}=10μF, C_{OUT}=10μF, T_A=25℃ , unless otherwise noted.)

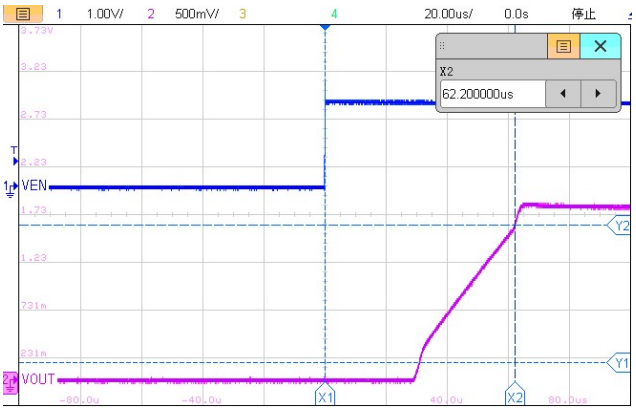
Parameter		Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Input Voltage		V_{IN}			2.7	--	20	V
Output Voltage Accuracy		ΔV_{OUT}	T_A=25°C		-2	--	+2	%
			T_A=-40°C ~ 85°C		-3	--	+3	%
Reference Voltage		V_{REF}			0.588	0.60	0.612	V
Quiescent Current		I_Q	I_{OUT}=0A		--	160	190	μA
Dropout Voltage		V_{DROP}	V_{OUT}=1.8V	I_{OUT}=1A, V_{IN} ≥ 2.7V, T_A=-40°C~125°C	--	750	800	mV
			V_{OUT}=3.3V		--	480	600	mV
			V_{OUT}=5.0V		--	450	550	mV
			V_{OUT}=1.8V	I_{OUT}=500mA, V_{IN} ≥2.7V, T_A=-40°C~125°C	--	650	900	mV
			V_{OUT}=3.3V		--	210	450	mV
			V_{OUT}=5.0V		--	200	400	mV
Line Regulation		ΔV_{LINE}	I_{OUT}=10mA, 2.8V ≤ V_{IN} ≤ 20V		--	0.05	0.2	%/V
Load Regulation		ΔV_{LOAD}	1mA≤ I_{OUT} ≤ 800mA, V_{IN}=V_{OUT}+1V		--	--	40	mV
Short Circuit/Start Carrying Current		I_{SHORT}	V_{OUT} = 0V		--	330	--	mA
Current Limit		I_{LIMIT}	V_{IN} =V_{OUT}+1V		1.04	1.3	--	A
Shutdown Current		I_{SHDN}	V_{EN}=0V		--	0.1	1	μA
Power Supply Rejection Ratio		PSRR	V_{IN}=V_{OUT}+2V I_{OUT}=50mA	f=1 KHz	--	80	--	dB
				f=100 KHz	--	70	--	dB
				f=1M KHz	--	65	--	dB
EN Input Threshold	Logic Low	V_{ENL}	EN Low Voltage		--	--	0.4	V
	Logic High	V_{ENH}	EN High Voltage		1.4	--	--	V
EN Pin Current		I_{EN}	V_{EN} ≤ V_{IN} ≤ 20V		--	1	--	μA
Output Noise Voltage		eN	V_{IN}= V_{OUT}+1V, I_{OUT}= 1mA, f=10Hz to100KHz, (V_{OUT}=3V), C_{OUT}=1μF		--	30*V_{OUT}	--	μV_{RMS}
Thermal Shut down Temperature		T_{SD}	Temperature Increasing from T_A=25°C		--	150	--	°C
Thermal Shutdown Hysteresis		T_{SDH}	Temperature Falling from T_{SD}		--	25	--	°C

Typical Electrical Curves

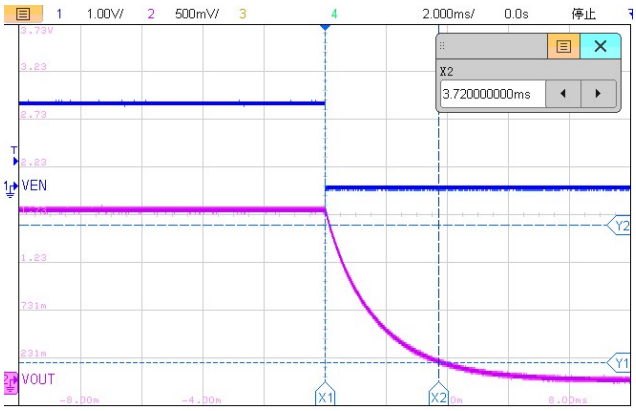
Test conditions: V_{IN} =V_{OUT}+1V , I_{OUT} =1mA ,C_{IN} =Ceramic 10μF, C_{OUT}=Ceramic 10μF(unless otherwise noted)

T_{ON} and T_{OFF}

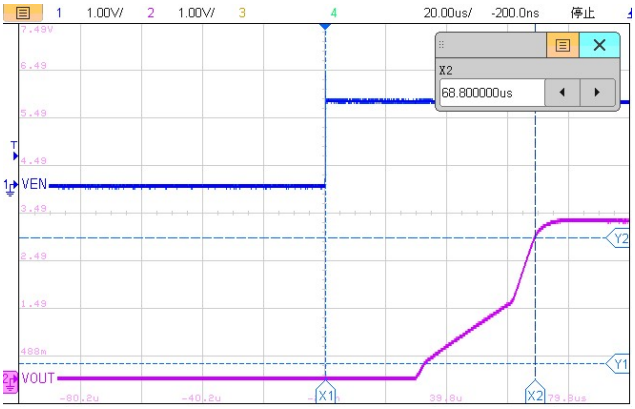
Turn On VS EN Voltage (V_{OUT}=1.8V, I_{OUT}=0mA)



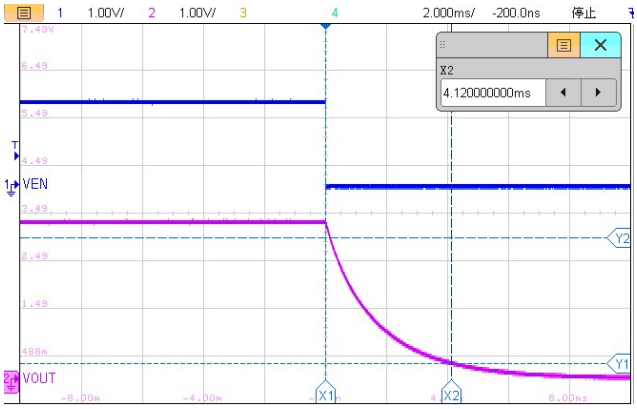
Turn Off VS EN Voltage (V_{OUT}=1.8V, I_{OUT}=0mA)



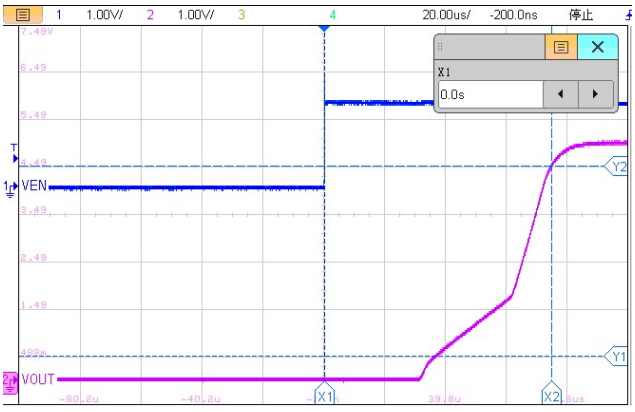
Turn On VS EN Voltage (V_{OUT}=3.3V, I_{OUT}=0mA)



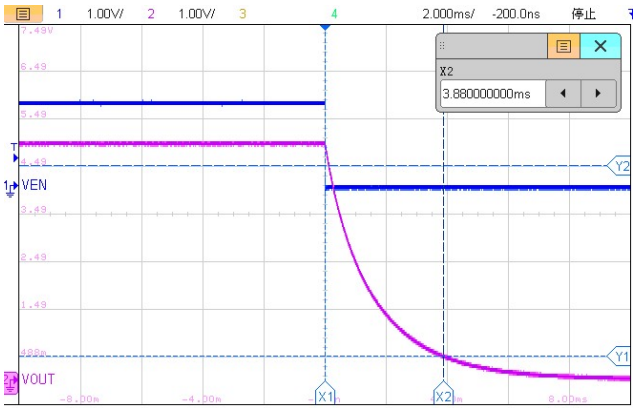
Turn Off VS EN Voltage (V_{OUT}=3.3V, I_{OUT}=0mA)



Turn On VS EN Voltage (V_{OUT}=5.0V, I_{OUT}=0mA)

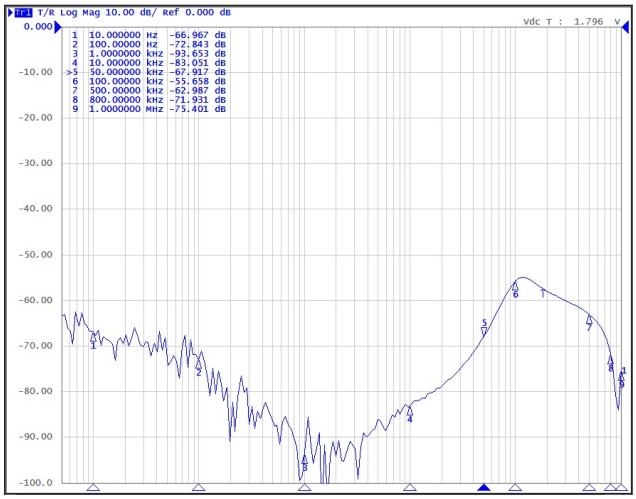


Turn Off VS EN Voltage (V_{OUT}=5.0V, I_{OUT}=0mA)

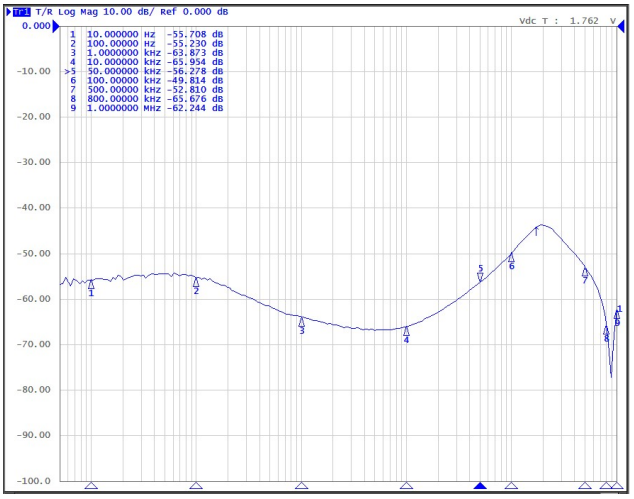


PSRR

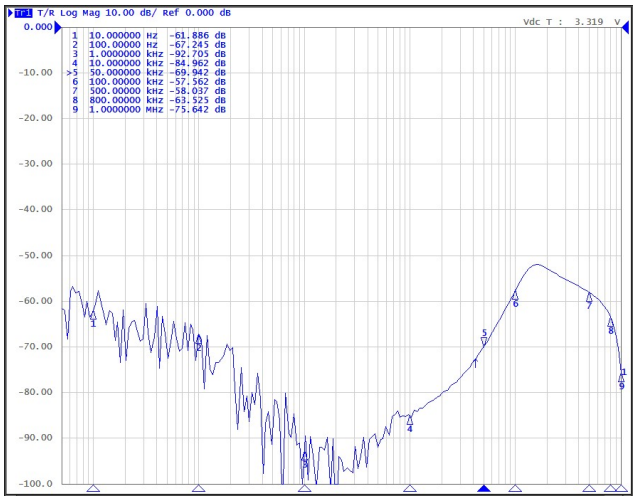
PSRR VS I_{OUT}(V_{OUT}=1.8V, I_{OUT}=50mA)



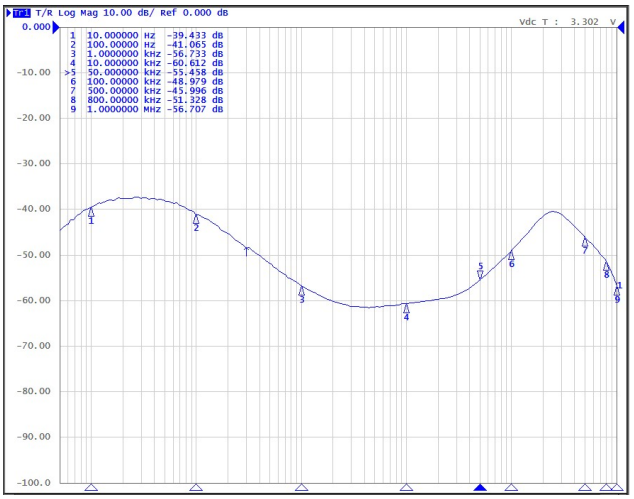
PSRR VS I_{OUT}(V_{OUT}=1.8V, I_{OUT}=500mA)



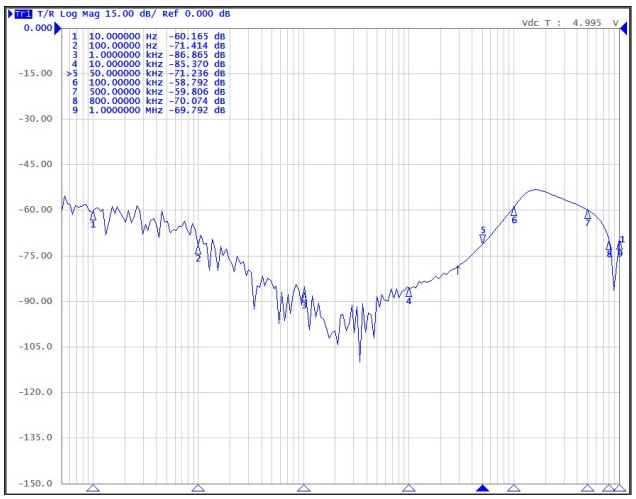
PSRR VS I_{OUT}(V_{OUT}=3.3V, I_{OUT}=50mA)



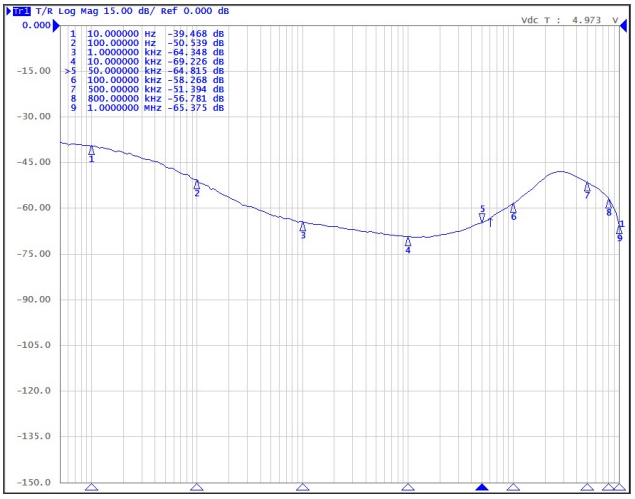
PSRR VS I_{OUT}(V_{OUT}=3.3V, I_{OUT}=500mA)



PSRR VS I_{OUT}(V_{OUT}=5.0V, I_{OUT}=50mA)



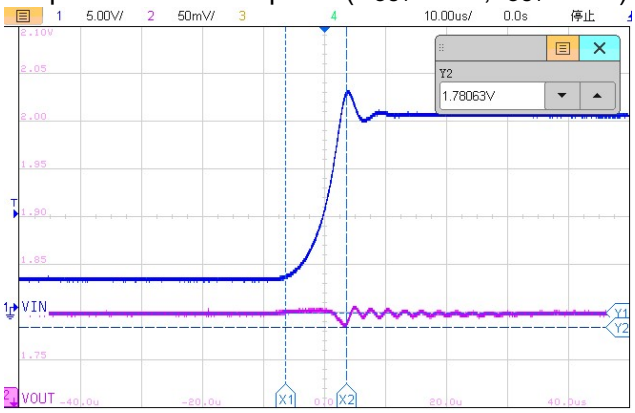
PSRR VS I_{OUT}(V_{OUT}=5.0V, I_{OUT}=500mA)



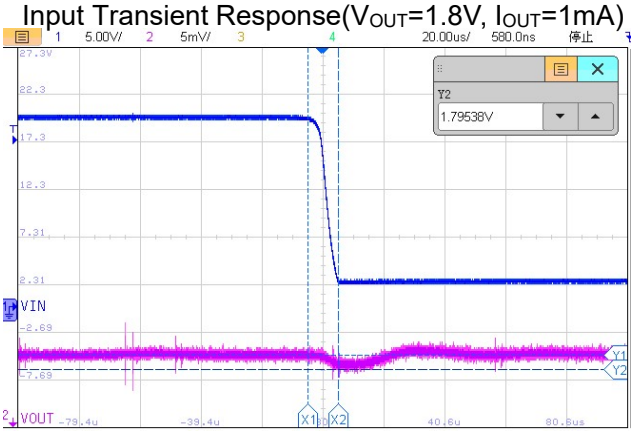
Input Transient Response

Test conditions: V_{IN} =V_{OUT}+1V , I_{OUT} =10mA ,t=10μS , C_{OUT}=10μF,V_{IN} jump from 6V to 18V

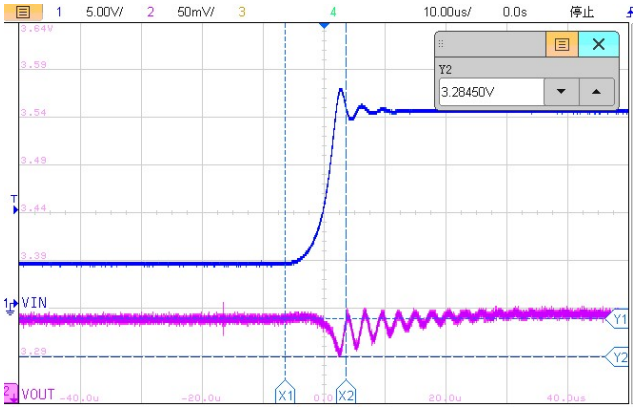
Input Transient Response(V_{OUT}=1.8V, I_{OUT}=1mA)



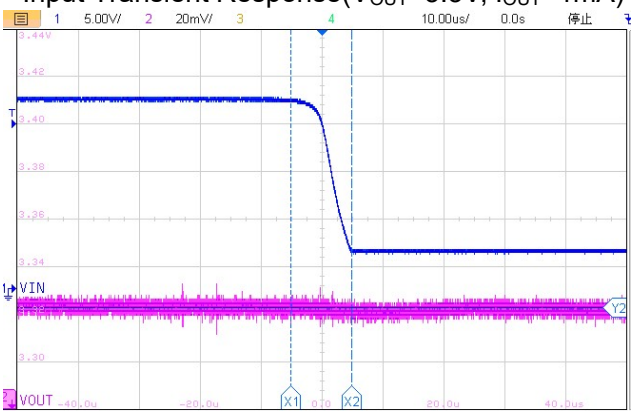
Input Transient Response(V_{OUT}=1.8V, I_{OUT}=1mA)



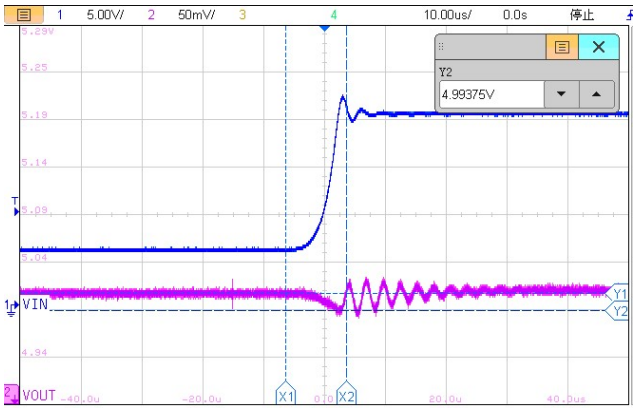
Input Transient Response(V_{OUT}=3.3V, I_{OUT}=1mA)



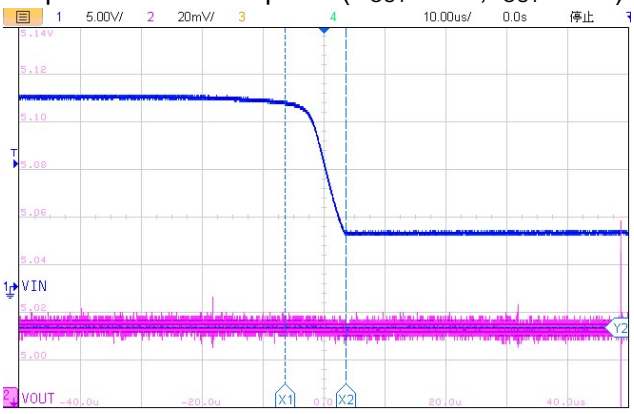
Input Transient Response(V_{OUT}=3.3V, I_{OUT}=1mA)



Input Transient Response(V_{OUT}=5.0V, I_{OUT}=1mA)



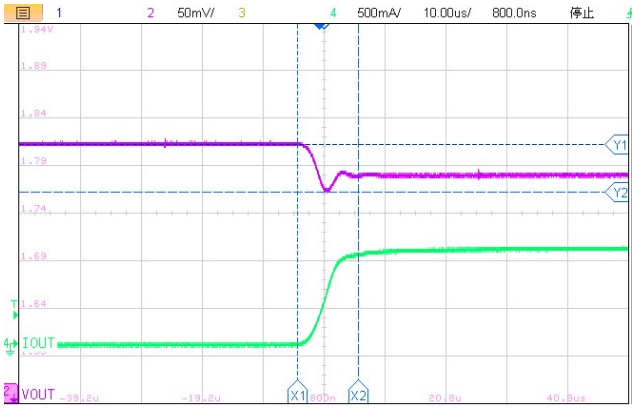
Input Transient Response(V_{OUT}=5.0V, I_{OUT}=1mA)



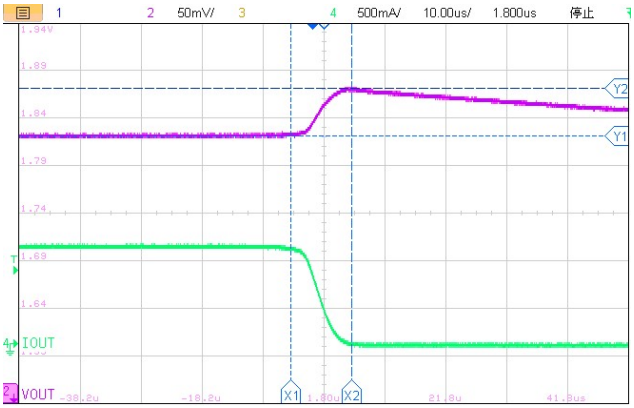
Load Transient Response

Test conditions: V_{IN} =V_{OUT}+1V, t=10μS, I_{OUT} jump from 1mA to 1000mA

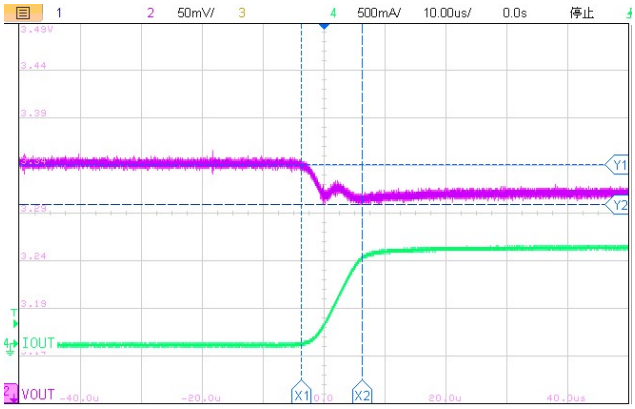
Load Transient Response(V_{OUT}=1.8V,I_{OUT}=1~1000mA)



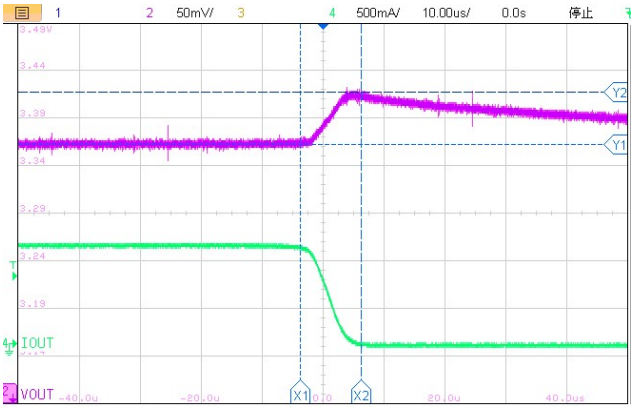
Load Transient Response(V_{OUT}=1.8V,I_{OUT}=1~1000mA)



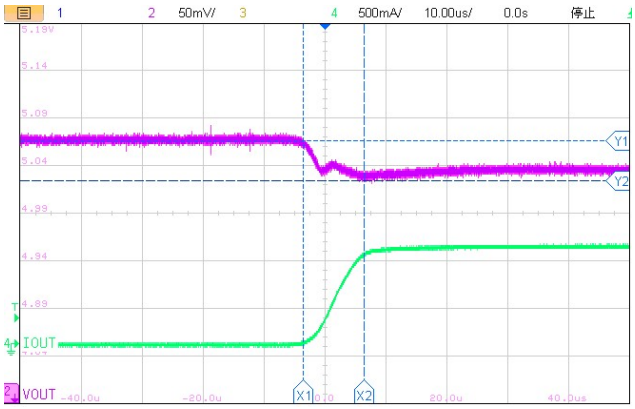
Load Transient Response(V_{OUT}=3.3V,I_{OUT}=1~1000mA)



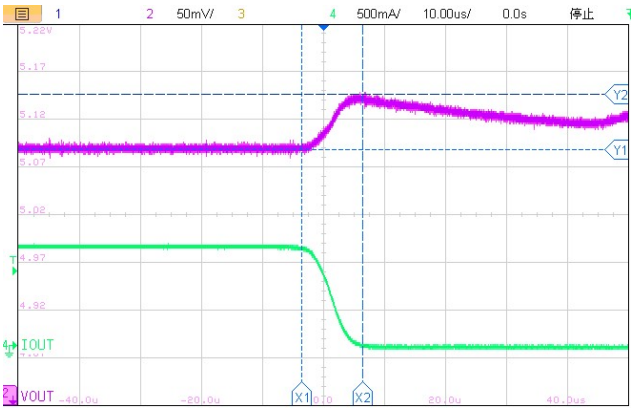
Load Transient Response(V_{OUT}=3.3V,I_{OUT}=1~1000mA)



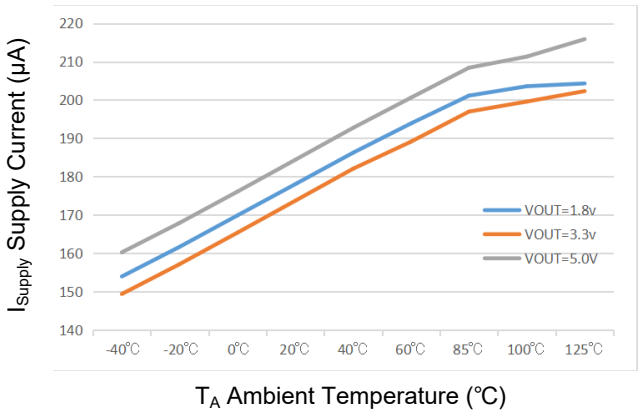
Load Transient Response(V_{OUT}=5.0V,I_{OUT}=1~1000mA)

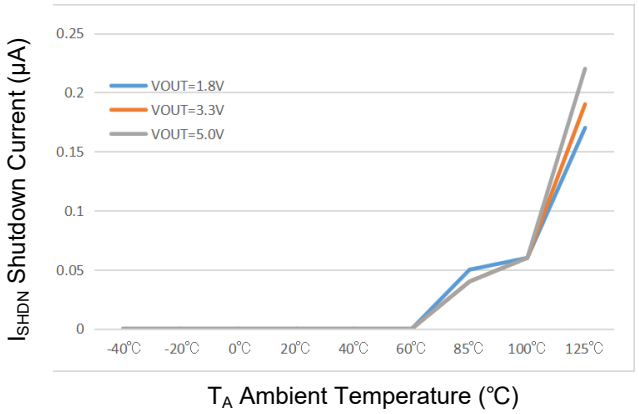


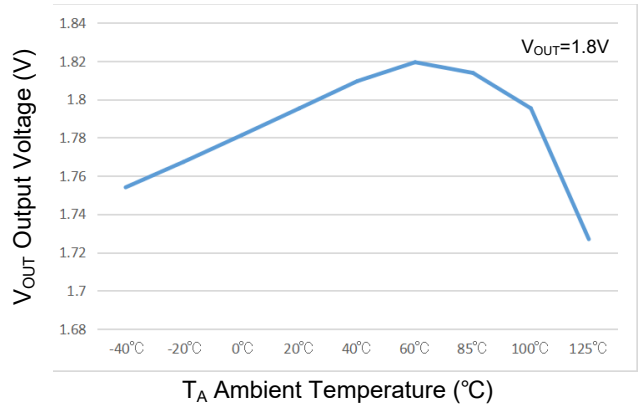
Load Transient Response(V_{OUT}=5.0V,I_{OUT}=1~1000mA)

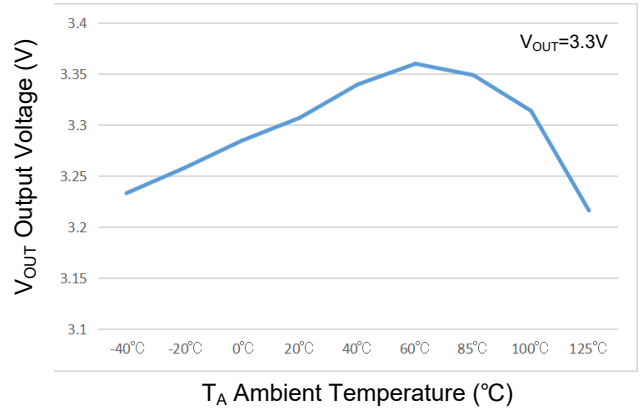


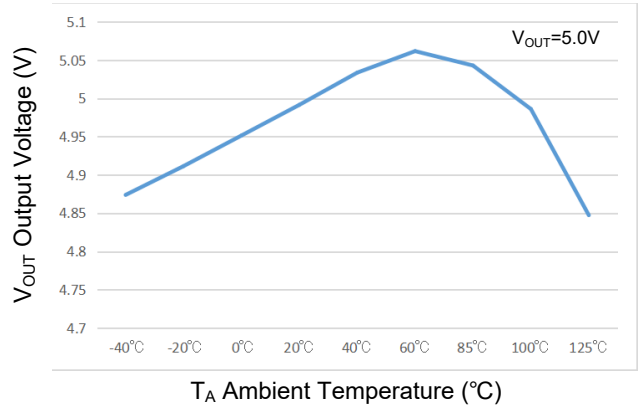
Temperature Characteristics











Application Information

Capacitor Selection

The TN51 Series requires an output capacitance of 4.7μF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application, pay attention to the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improve stransient response, input ripple, and PSRR. If the input supply has a high impedance over a large range off requencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

Application of Electrolytic Capacitor

If the electrolytic capacitor should be used as input and output capacitor, the capacitance of the capacitor must be greater. The capacity value must be greater than 22uF.

Enable

The TN51 Series has an EN pin to turn on or turn off the regulator, When the EN pin is in logic high, the regulator will be turned on. The shutdown current is almost 0uA typical. The EN pin may be directly tied to V_{IN} to keep the part on. The Enable input is CMOS logic and cannot beleft floating.

Setting the Output Voltage

The TN51 Series develops a 0.6V reference voltage, V_{REF}, between the output and the adjust terminal. This voltage is applied across resistor R1 to generate a constant current. The current I_{ADJ} from the ADJ terminal could introduce DC offset to the output. Because, this offset is very small (about 0.1 uA), it can be ignored. The constant current then flows through the output set resistor R2 and sets the output voltage to the desired level. Equation 2 is used for calculating V_{OUT}:

$$V_{OUT} = 0.6V \times (1 + R1 / R2)$$

Although I_{ADJ} is very small, R1+R2 should be limited to less than 100 KΩ for optimum performance.

Dropout Voltage

The TN51 Series uses a PMOS pass transistor to achieve low dropout. When ($V_{IN} – V_{OUT}$) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as ($V_{IN} – V_{OUT}$) approaches dropout operation.

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 150°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 125°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the ($V_{IN} – V_{OUT}$) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$$

Where $T_{J(MAX)}$ is the maximum junction temperature of the die (150°C), Ta is the maximum ambient temperature,and $R_{\theta JA}$ is the junction to ambient thermal resistance.

For recommended operating condition specifications the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, $R_{\theta JA}$, is layout dependent. For DFN2x2C-6L package, the thermal resistance, $R_{\theta JA}$, is 80°C/W on the test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula:

$$P_{D(MAX)} = (125°C - 25°C) / (80°C/W) = 1.25W \text{ for DFN2x2C-6L package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, $R_{\theta JA}$. in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

Layout

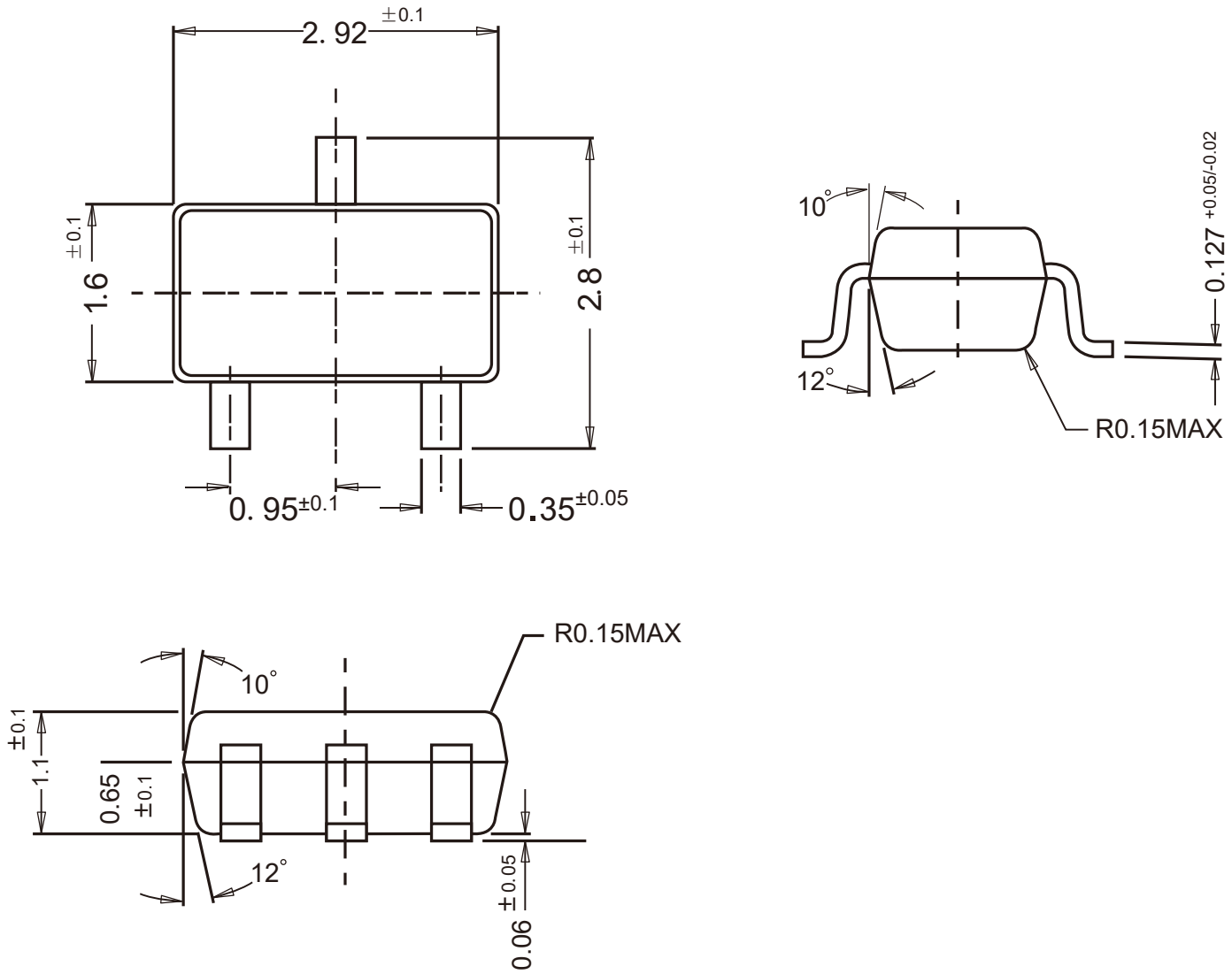
Layout Guidelines

1. Place input and output capacitors as close to the device as possible.
2. Use copper planes for device connections in order to optimize thermal performance.
3. Place thermal vias around the device to distribute heat.
4. Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

Package Outline

SOT-23-3

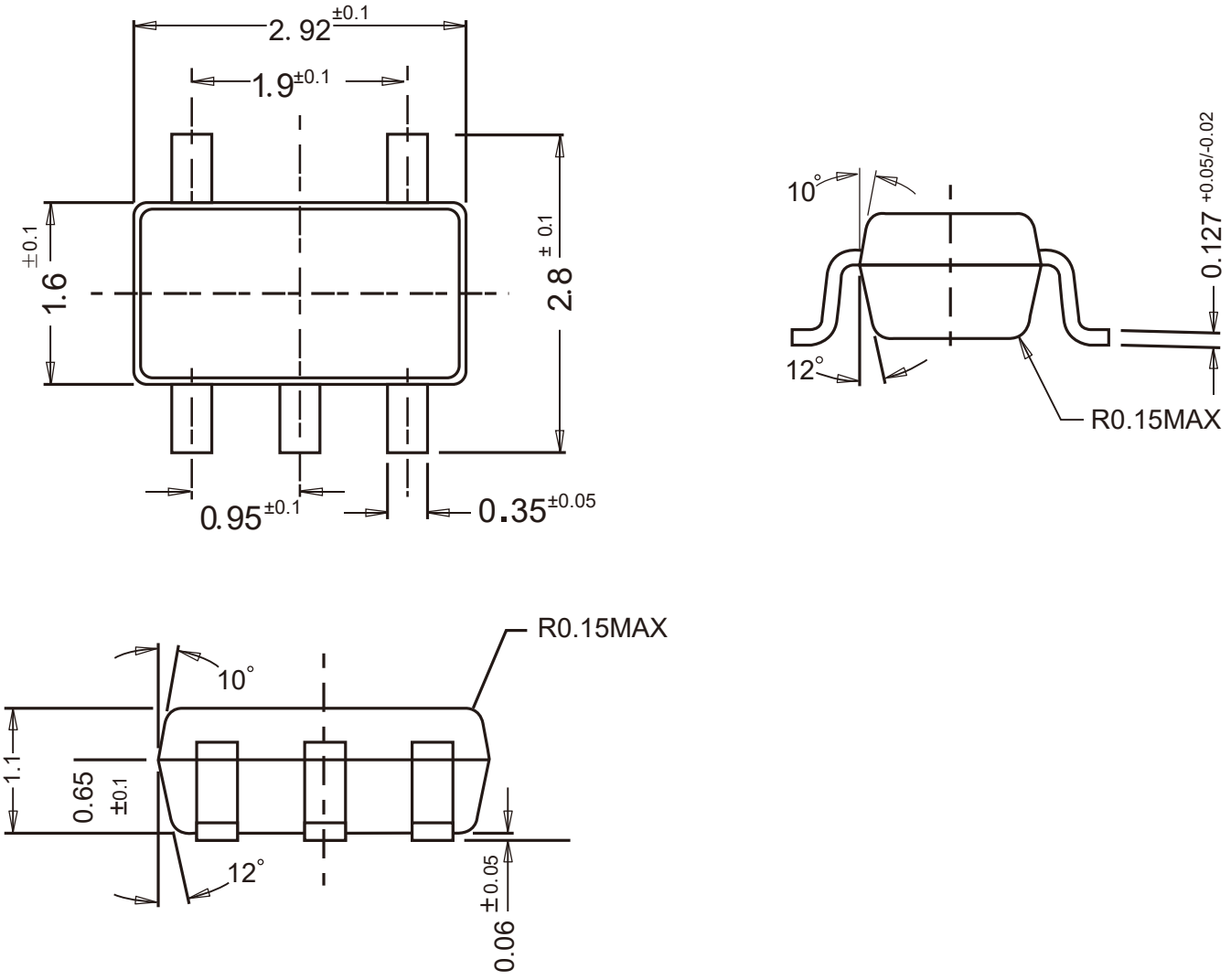
Dimensions in mm



Package Outline

SOT-23-5

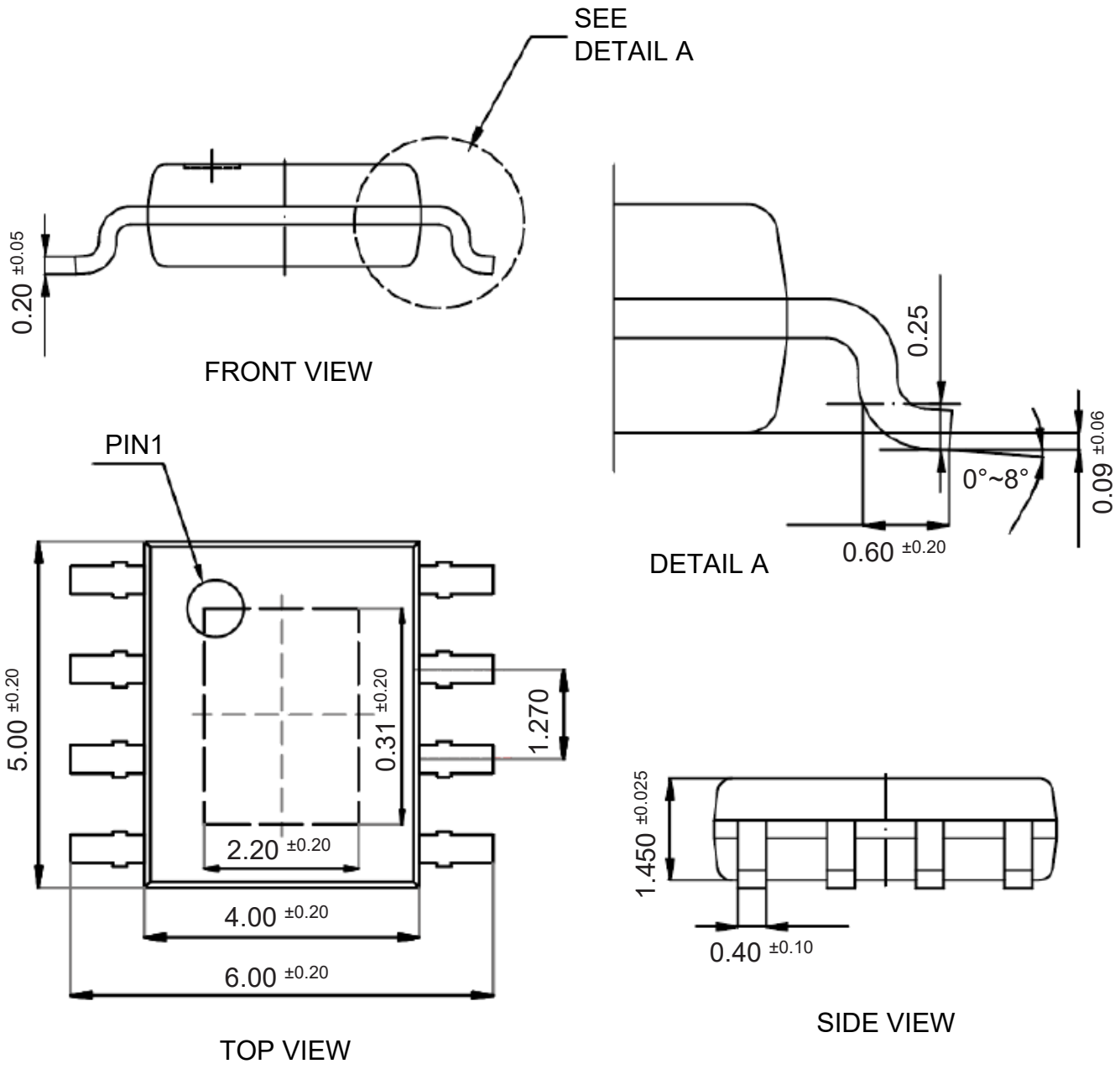
Dimensions in mm



Package Outline

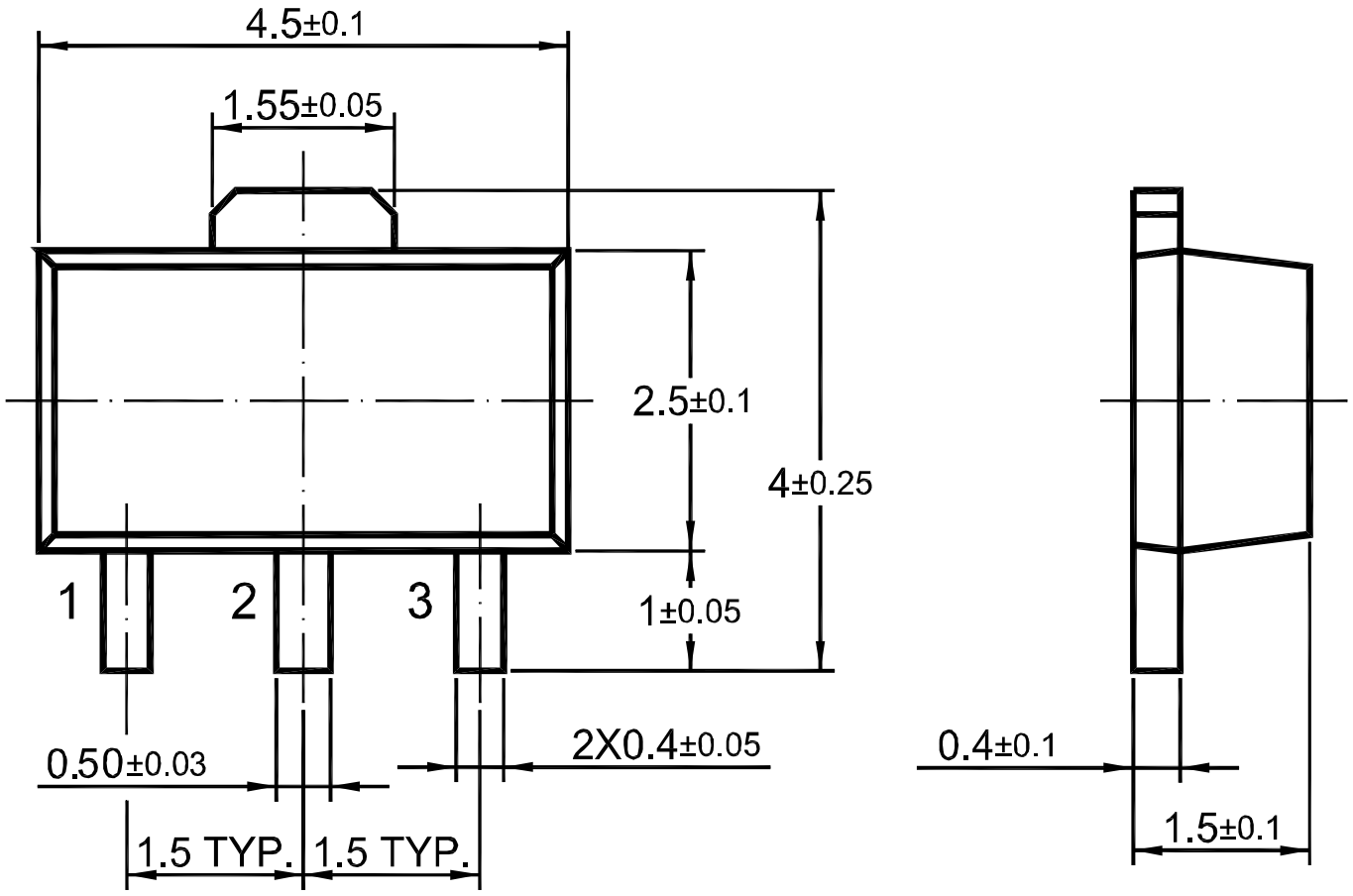
ESOP-8

Dimensions in mm



Package Outline

SOT-89 Dimensions in mm



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For additional information, please contact your local Sales Representative.

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