TL494 Switch Mode Power Supply Controller

Description

UTusemi

The TL494 is used for the control circuit of the PWM switching regulator, The TL494 consists of 5V reference voltage circuit, two error amplifiers, flip flop, an output control circuit, a PWM comparator, a dead time comparator and an oscillator. This device can be operated in the switching frequency of 1 KHz to 300 KHz.

Features

- Internal regulator provides a stable 5V reference supply trimmed to 5%
- Uncommitted output TR for 200mA sink or source current
- Output control for push-pull or single-ended operation
- Variable duty cycle by deadtime control (pin 4)Complete PWM control circuit
- On-chip oscillator with master or slave operation
- Internal circuit prohibits double pul se at either output





A5L=AIA F5H=B; Gft i ```cdYfUh]b['Ua V]YbhhYa dYfUhifY'fUb[Y'Udd`]Ygzi b`Ygg'ch Yfk]gY'bchYX'Ł

Rating	Symbol	TL494C	TL494I	Unit
Power Supply Voltage	VCC	4	2	V
Collector Output Voltage	V _{C1} , V _{C2}	42		V
Collector Output Current (Each transistor) (Note 1)	IC1, IC2	500		mA
Amplifier Input Voltage Range	VIR	-0.3 to +42		V
Power Dissipation @ $T_A \le 45^{\circ}C$	PD	1000		mW
Thermal Resistance, Junction–to–Ambient	R _θ JA	80		°C/W
Operating Junction Temperature T _J		12	25	°C
Storage Temperature Range	T _{stg}	–55 to	+125	°C
Operating Ambient Temperature Range TL494C TL494I	TA	0 to –25 t	+70 o +85	°C
Derating Ambient Temperature	ТА	45		°C



NOTE: Maximum thermal limits must be observed

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Тур	Max	Unit
Power Supply Voltage	V _{CC}	7.0	15	40	V
Collector Output Voltage	V _{C1} , V _{C2}	-	30	40	V
Collector Output Current (Each transistor)	IC1, IC2	-	-	200	mA
Amplified Input Voltage	V _{in}	-0.3	-	V _{CC} – 2.0	V
Current Into Feedback Terminal	lfb	_	-	0.3	mA
Reference Output Current	l _{ref}	_	-	10	mA
Timing Resistor	RT	1.8	30	500	kΩ
Timing Capacitor	CT	0.0047	0.001	10	μF
Oscillator Frequency	f _{osc}	1.0	40	200	kHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μ F, R_T = 12 k Ω , unless otherwise noted.) For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Тур	Max	Unit
REFERENCE SECTION					
Reference Voltage (I _O = 1.0 mA)	V _{ref}	4.75	5.0	5.25	V
Line Regulation (V _{CC} = 7.0 V to 40 V)	Reg _{line}	-	2.0	25	mV
Load Regulation (I _O = 1.0 mA to 10 mA)	Regload	-	3.0	15	mV
Short Circuit Output Current (V _{ref} = 0 V)	ISC	15	35	75	mA
OUTPUT SECTION	•	•			
Collector Off–State Current (V _{CC} = 40 V, V _{CE} = 40 V)	^I C(off)	-	2.0	100	μΑ
Emitter Off–State Current $V_{CC} = 40 V, V_{C} = 40 V, V_{E} = 0 V$	lE(off)	-	-	-100	μΑ
Collector–Emitter Saturation Voltage (Note 2) Common–Emitter ($V_E = 0 V$, $I_C = 200 mA$) Emitter–Follower ($V_C = 15 V$, $I_E = -200 mA$)	V _{sat(C)} V _{sat(E)}		1.1 1.5	1.3 2.5	V
$\begin{array}{l} \text{Output Control Pin Current} \\ \text{Low State } (V_{OC} \leq 0.4 \text{ V}) \\ \text{High State } (V_{OC} = V_{ref}) \end{array}$	IOCL IOCH		10 0.2	_ 3.5	μA mA
Output Voltage Rise Time Common–Emitter (See Figure 12) Emitter–Follower (See Figure 13)	t _r	-	100 100	200 200	ns
Output Voltage Fall Time Common–Emitter (See Figure 12) Emitter–Follower (See Figure 13)	t _f		25 40	100 100	ns

NOTE: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

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ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μ F, R_T = 12 k Ω , unless otherwise noted.) For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Тур	Max	Unit	
ERROR AMPLIFIER SECTION						
Input Offset Voltage (V _{O (Pin 3)} = 2.5 V)	V _{IO}	_	2.0	10	mV	
Input Offset Current (V _{O (Pin 3)} = 2.5 V)	lio	_	5.0	250	nA	
Input Bias Current (V _O (Pin 3) = 2.5 V)	IIB	_	-0.1	-1.0	μA	
Input Common Mode Voltage Range (V _{CC} = 40 V, T _A = 25°C)	VICR	-	-0.3 to V _{CC} -2	.0	V	
Open Loop Voltage Gain (ΔV_O = 3.0 V, V _O = 0.5 V to 3.5 V, R _L = 2.0 k Ω)	AVOL	70	95	_	dB	
Unity–Gain Crossover Frequency (V _O = 0.5 V to 3.5 V, R _L = 2.0 k Ω)	fC-	_	350	_	kHz	
Phase Margin at Unity–Gain (V _O = 0.5 V to 3.5 V, R _L = 2.0 k Ω)	[¢] m	_	65	_	deg.	
Common Mode Rejection Ratio (V _{CC} = 40 V)	CMRR	65	90	_	dB	
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V _O = 2.5 V, R _L = 2.0 k Ω)	PSRR	_	100	_	dB	
Output Sink Current (V _{O (Pin 3)} = 0.7 V)	IO-	0.3	0.7	_	mA	
Output Source Current (VO (Pin 3) = 3.5 V)	IO+	2.0	-4.0	_	mA	
PWM COMPARATOR SECTION (Test Circuit Figure 11)			1			
Input Threshold Voltage (Zero Duty Cycle)	V _{TH}	_	2.5	4.5	V	
Input Sink Current (V _(Pin 3) = 0.7 V)	II_	0.3	0.7	_	mA	
DEADTIME CONTROL SECTION (Test Circuit Figure 11)						
Input Bias Current (Pin 4) (VPin 4 = 0 V to 5.25 V)	IIB (DT)	_	-2.0	-10	μA	
Maximum Duty Cycle, Each Output, Push–Pull Mode (V _{Pin 4} = 0 V, C _T = 0.01 μF, R _T = 12 kΩ)	DC _{max}	45	48	50	%	
$(V_{Pin 4} = 0 V, C_T = 0.001 \mu F, R_T = 30 k\Omega)$		-	45	50		
Input Threshold Voltage (Pin 4)	V _{th}		2.0	2.2	V	
(Maximum Duty Cycle)		0	2.0	3.3		
OSCILLATOR SECTION						
Frequency (C _T = 0.001 μ F, R _T = 30 k Ω)	f _{osc}	_	40	_	kHz	
Standard Deviation of Frequency* (C _T = 0.001 μ F, R _T = 30 k Ω)	σf _{osc}	_	3.0	_	%	
Frequency Change with Voltage (V _{CC} = 7.0 V to 40 V, T _A = 25°C)	$\Delta f_{OSC} (\Delta V)$	_	0.1	_	%	
Frequency Change with Temperature ($\Delta T_A = T_{low}$ to T_{high}) (C _T = 0.01 µF, R _T = 12 kΩ)	$\Delta f_{OSC} (\Delta T)$	-	-	12	%	
UNDERVOLTAGE LOCKOUT SECTION			1			
Turn–On Threshold (V _{CC} increasing, I _{ref} = 1.0 mA)	V _{th}	5.5	6.43	7.0	V	
TOTAL DEVICE	1		1			
Standby Supply Current (Pin 6 at V _{ref} , All other inputs and outputs open) (V _{CC} = 15 V)	ICC	_	5.5	10	mA	
(V _{CC} = 40 V)		_	7.0	15		
Average Supply Current (CT = $0.01 \mu\text{F}$, RT = $12 k\Omega$, V(Pin 4) = 2.0V) (V _{CC} = 15V) (See Figure 12)		_	7.0	_	mA	

* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \frac{\sqrt{\sum_{n=1}^{N} (X_n - \overline{X})^2}}{\sqrt{\frac{n=1}{N-1}}}$





Figure 1. Representative Block Diagram

This device contains 46 active transistors.



Figure 2. Timing Diagram

Description

The TL494 is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal–linear sawtooth oscillator is frequency–programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{OSC} \approx \frac{1.1}{RT \bullet CT}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip–flop clock–input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control–signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first 4% of the sawtooth–cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime–control input to a fixed voltage, ranging between 0 V to 3.3 V.

Input/Output Controls	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single–ended PWM @ Q1 and Q2	1.0
@ Vrof	Push-pull Operation	0.5

Functional Table

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from -0.3 V to (V_{CC} - 2V), and

may be used to sense power–supply output voltage and current. The error–amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor CT is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of $\pm 5.0\%$ with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C.



Figure 3. Oscillator Frequency versus Timing Resistance

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Phase versus Frequency 120 AVOL, OPEN LOOP VOLTAGE GAIN (dB) 1 2 3 9 3 90 12 8 06 00 11 1 $V_{CC} = 15 V_{\Delta} V_{O} = 3.0 V_{RL} = 2.0 k\Omega^{-1}$ 0 20 AVOL 60 80 140 _ 160 0 180 1.0 10 100 1.0 k 10 k 100 k 1.0 M f, FREQUENCY (Hz)

Figure 4. Open Loop Voltage Gain and

Figure 5. Percent Deadtime versus Oscillator Frequency



Figure 6. Percent Duty Cycle versus Deadtime Control Voltage



Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current



Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current







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Figure 10. Error–Amplifier Characteristics



Figure 11. Deadtime and Feedback Control Circuit

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Figure 12. Common–Emitter Configuration Test Circuit and Waveform



Figure 13. Emitter–Follower Configuration Test Circuit and Waveform



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Figure 10. Error–Amplifier Characteristics



Figure 11. Deadtime and Feedback Control Circuit



Figure 12. Common–Emitter Configuration Test Circuit and Waveform





Figure 13. Emitter–Follower Configuration Test Circuit and Waveform





Figure 14. Error-Amplifier Sensing Techniques







Figure 16. Soft-Start Circuit



Figure 17. Output Connections for Single–Ended and Push–Pull Configurations



Figure 18. Slaving Two or More Control Circuits



Figure 19. Operation with V_{in} > 40 V Using External Zener



Figure 20. Pulse Width Modulated Push-Pull Converter



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Test	Conditions	Results
Line Regulation	V _{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I _O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V _{in} = 28 V, I _O = 1.0 A	65 mV pp P.A.R.D.
Short Circuit Current	V _{in} = 28 V, R _L = 0.1 Ω	1.6 A
Efficiency	V _{in} = 28 V, I _O = 1.0 A	71%

- L1 3.5 mH @ 0.3 A T1 – Primary: 20T C.T. #28 AWG Secondary: 12OT C.T. #36 AWG
 - Core: Ferroxcube 1408P-L00-3CB



Figure 21. Pulse Width Modulated Step–Down Converter

Test	Conditions	Results	
Line Regulation	V _{in} = 8.0 V to 40 V	3.0 mV 0.01%	
Load Regulation	V_{in} = 12.6 V, I _O = 0.2 mA to 200 mA	5.0 mV 0.02%	
Output Ripple	V _{in} = 12.6 V, I _O = 200 mA	40 mV pp P.A.R.D.	
Short Circuit Current	V_{in} = 12.6 V, R _L = 0.1 Ω	250 mA	
Efficiency	V _{in} = 12.6 V, I _O = 200 mA	72%	

OUTLINE DIMENSIONS



Contact Information

TANI website: http://www.tanisemi.com Email:tani@tanisemi.com

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